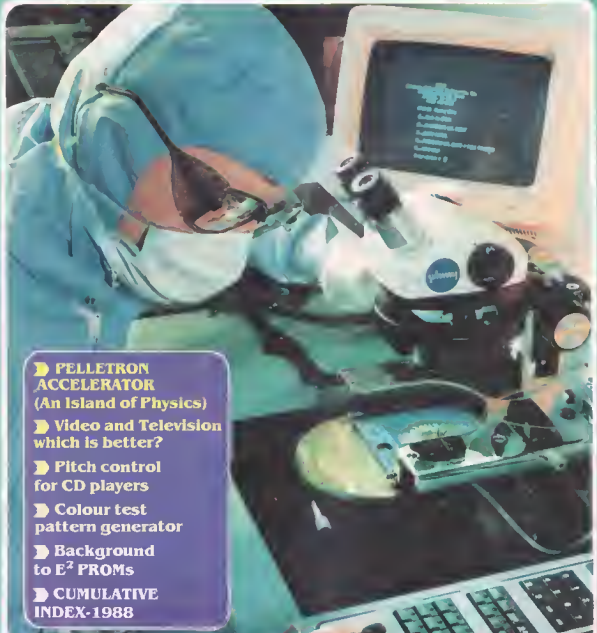


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- 
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(An Island of Physics)
 - **Video and Television**
which is better?
 - **Pitch control**
for CD players
 - **Colour test**
pattern generator
 - **Background**
to E^2 PROMs
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TOWARDS THE INTELLIGENT HOUSE

The rapid growth of electronics inspires us to take a look at what changes we are likely to see in domestic environments of the future.

Homes will be equipped increasingly with a domestic computer terminal (put in by the builders like a sink unit). This will control the central heating, hot water supply, cooker, video, lighting, and so on. Eventually, there will be a fully automated kitchen that will carry out most of the irksome tasks like ironing and washing up.

This domestic computer will be controlled via the public telephone network. The conventional telephone will be replaced by a wristwatch type, so that the home can be controlled from wherever you are.

The conventional door lock will disappear and be replaced by tone-detecting electronic locks that respond to the householders' voices.

Although the combustion-engine-driven car will not disappear for a long time to come, there will be an increasing number of electric cars. New, small, large-capacity batteries will make these a commercially viable proposition. All cars will be fitted with a large number of electronic gadgets to take the tediousness out of driving. They will have microprocessors that control fuel injection, gear changing, spring rate, vehicle height, shock absorber damping, and others. All cars will be equipped with anti-brake-lock systems and sensors that actuate the braking system when you get too close to the car in front.

Increasingly, shopping will be done from home with the aid of video-telephones and electronic fund transfer.

Home entertainment will be based on digital equipment, and probably be interactive, allowing subscriber selection of high-definition, 3D, large-screen, video, television, and music via common networks.

Television and video communications will dominate the home even more than they do now. With more and more satellites hovering above the equator, signals from them will be received via dishes not much larger than a dinner plate. The screens will be linked in with the telephone network so that all communications will be face-to-face.

Cellular radio systems, linked world-wide by satellite systems will be commonplace so that anyone can communicate with anybody else wherever they may be.

Paraplegics may be able to walk again with the aid of electrical stimulation of their muscles. These stimuli will come from pressure, angular, and acceleration sensors on their limbs.

The deaf will have portable videophones in which a microprocessor displays the incoming telephone speech on to a screen.

Electronic devices will continue to get smaller and faster, although the size of finished products will, of course, still be dictated by the needs of the user. Slowly but surely, silicon ICs will be replaced by gallium-arsenide chips, and these, in turn, will be superseded by neural or optical devices. The density of these devices will be staggering by current standards.

The future certainly looks exciting, the more so for those of us who play an active part in the wonderful world of electronics!

Front cover

The design of microcircuits is becoming more challenging every year. Plessey's Rotherham silicon wafer fabrication plant in Plymouth produces CMOS chips that require much less power than other types and are particularly suited to telecommunications, computers, traffic controls and robots. Completed wafers are subjected to comprehensive testing to guarantee performance and to provide data for process control.

BUS INTERFACE FOR HIGH-RESOLUTION LIQUID CRYSTAL SCREENS

Part 2

Construction

The LC screen interface is constructed on a double-sided, through-plated printed circuit board (see Fig. 4). The track layout is not given here because this PCB is virtually impossible to make other than from films, while through-plating equipment is usually only available in a professional workshop. The size of the ready-made PCB is such that it can be attached to the controller board of the LM40001 unit with the aid of 4 spacers. The connection between the interface board and the existing controller board is conveniently made in a short length of 10-way flat ribbon cable. The mounting of the standard-sized components on the board should not present difficulties. Only the controller, IC₁, deserves special attention. This IC is housed in a 64-pin flatpack enclosure for surface mounting, with pins in a 1 mm, rather than a 0.1 in., raster. Use a low-power soldering iron with a small tip to solder the terminal pins of the controller direct on to the relevant copper tracks. Work very carefully, and use desoldering braid to remove solder when a short-circuit is made between adjacent pins. As to orientation of the controller chip on the board, stick to the component overlay, because pin 1 is not located immediately next to the bevelled edge of the enclosure!

Connector K₁, a 40-way PCB header with ejection handles, is secured on to the PCB by means of two small bolts and nuts. The pinning of K₁ makes it possible to use a direct, pin-to-pin, connection, in flatcable, to the expansion connector on the BASIC computer ⁽¹⁾. For other computer systems, it is necessary to provide a do-it-yourself connection between K₁ and the bus (see Tables 3a and 3b). Whatever connection is used, the total length of the cable between the computer bus and K₁ should not exceed 30 cm or so.

Programming the LC screen interface

Software for producing ASCII characters on the LC screen is relatively simple to produce thanks to the con-

Table 2 Interface configuration data

Processor	Z80* (MSX)				6502		IBM-PC*		ELEKTOR BASIC COMPUTER	
Jumpers	A,C,E,G,I,K,Q,T				A,B,H,L,P,S		C,D,F,M,Q		C,D,F,M,P,S	
Mapping	I/O				MEMORY		I/O		MEMORY	
k1										
X0	S1	M1	off	—	off	AEN	on	—	off	
X1	S2	—	off	—	off	A3	X	—	off	
X2	S3	—	off	—	off	A4	X	—	off	
A3-A5	S4-S6	A3-A5	X	A3-A5	X	A5-A7	on	A3-A5	X	
A6-A7	S7-S9	A6-A7	X	A6-A7	X	A8-A9	off	A6-A7	X	
				(MSX ON)						
A8-A15	S10-S16	—	—	A8-A15	X	—	—	A8-A15	X	
Address range		MSX 0-3FH else 00-FFH		system dependent		300H-31FH		system- dependent		
		X2—IOREQ X1—MI RST—RESET WAIT—WAIT for MSX: PHIZ/DIR—BUSDIR SW1 SW2		PHIZ/DIR—Q 2 RST—NRST WR—RD/WR		X0—AEN RST—RESET WAIT—IOCHROY RD—IORQ WR—IOWR		—		

*IC6, S9-S16 and R2 may be omitted

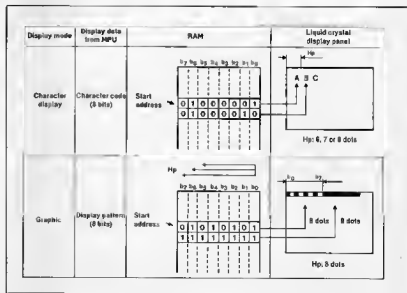


Fig. 6. Difference between character (text) display and graphic display mode as regards processing of individual bits loaded from the screen RAM.

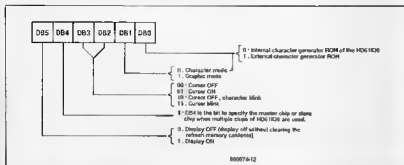


Fig. 5. Bit assignment in the MODE register of the LCD controller.

Table 3a

SLOT		←	SIGNAL DESCRIPTION
PIN NO.	NAME	I/O	DESCRIPTION
1	CS1	O	ROM 4000 ~ 7FFF select signal (128K)
2	CS2	O	ROM 8000 ~ BFFF select signal (128K)
3	CS12	O	ROM 4000 ~ BFFF select signal (256K)
4	SLTSL	O	Slot selected signal. ← Fixed select signal for each slot.
5		—	Reserved for future use
6	RFSH	O	Refresh signal
7	WAIT	I	Wait for signal to CPU (wired-OR)
8	INT	I	Interrupt request signal
9	M1	O	Fetch cycle signal of CPU
10	BUSDIR	I	This signal controls the direction of external data bus buffer when the cartridge is selected. It is low level when the data is sent by the cartridge.
11	IORG	O	I/O request signal
12	MERG	O	Memory request signal
13	WR	O	Write signal
14	RD	O	Read signal
15	RESET	O	System reset signal
16		—	Reserved for future use
17	A9	O	Address bus
18	A15	O	
19	A11	O	
20	A10	O	
21	A7	O	
22	A6	O	
23	A12	O	
24	A8	O	
25	A14	O	Data bus
26	A13	O	
27	A1	O	
28	A0	O	
29	A3	O	
30	A2	O	
31	A5	O	
32	A4	O	
33	O1	I/O	Data bus
34	O0	I/O	
35	O3	I/O	
36	O2	I/O	
37	O5	I/O	
38	O4	I/O	
39	O7	I/O	
40	O6	I/O	
41	GND	—	Ground
42	CLOCK	O	
43	GND	—	
44, 46	SW1, SW2	—	
45, 47	+5 V	—	
48	+12 V	—	
49	SOUND IN	I	
50	-12 V	—	

Input and output refers to MSX computer

Table 3b Signal functions on IBM bus

Signal name		Signal Name
GND	B1	A1 -I/O CH CK
+RESET DRV	B2	A2 +D7
+5V	B3	A3 +D6
+IRQ2	B4	A4 +D5
-SVDC	B5	A5 +D4
+DRQ2	B6	A6 +D3
-12V	B7	A7 +D2
Reserved	B8	A8 +D1
+12V	B9	A9 +D0
GND	B10	A10 -I/O CH RDY
-MEMW	B11	A11 +AEN
MEMR	B12	A12 +A19
-IOW	B13	A13 +A18
-IOR	B14	A14 +A17
-DACK3	B15	A15 +A16
+DRQ3	B16	A16 +A15
-DACK1	B17	A17 +A14
+DRQ1	B18	A18 +A13
-DACK0	B19	A19 +A12
CLOCK	B20	A20 +A11
+IRQ7	B21	A21 +A10
+IRQ5	B22	A22 +A9
+IRQ5	B23	A23 +A8
+IRQ4	B24	A24 +A7
+IRQ3	B25	A25 +A6
-DACK2	B26	A26 +A5
+Y/C	B27	A27 +A4
+ALE	B28	A28 +A3
+5V	B29	A29 +A2
+DSC	B30	A30 +A1
+GND	B31	A31 +A0

troller taking over the task of generating the dot patterns for the characters. Briefly recapitulating what has been said in the above description of the circuit, the five registers of Table 1 are either read or write locations. Four of these registers control the HD61830B, and one, LATCH, IC₁₁, whose output state determines the contrast (bits 0 to 3), the selected 4 Kbyte screen RAM (bit 6), and the selected add-on character font (bit 7).

Table 4 shows that the controller chip offers quite a few programmable functions. Its basic operation will be discussed with a few examples as guidance for further developments.

To start with, it is seen that the chip has 14 registers for storing different parameters. One register, number 14, returns the busy flag, which is logic high for about 15 μ s after receipt of a controller command. The controller can not handle a new command as long as the busy flag is active. Busy can be read from the databus via register CTRL-RD (control read). It will be clear that there is very little point in using this flag in BASIC, because the relatively low processing speed of this programming language makes it impossible anyway to send a new command to the controller before this has deactivated the busy flag. Machine code programmers, however, are well advised to have the control program read and process the busy flag.

Before any character can be displayed on the LC screen, the controller must be in

itized. For the following description it is assumed that an LC screen Type LM40001 is used. For other types, the relevant data sheets should be examined to analyse the register assignment.

The first 4 registers in the HD61830B should always be loaded. Table 4 shows that register 0 is the mode control. The various options available are given in Fig. 5. Writing to a register is done in two passes: first, load the register number in address control-write (CTRL-WR), then write the relevant data to address data-write (DATA-WR). The BASIC listing of Fig. 9 illustrates this procedure. The subroutine starting at line 1000 loads variable DA in register CTL. The other four registers are loaded in a similar fashion.

Lines 60 to 100 in the demonstration program hold the data for loading controller registers R0 up to and including R4. The corresponding screen settings form a usable default configuration, and are best copied for initial experiments in programming the LC screen. It is possible to read the data at the cursor address. To do this, first load the required cursor address in register 7 (LS byte) and register 8 (MS byte). Then perform a dummy read via address DATA-RD. Next, read the data 'underneath' the cursor from address DATA-RD. Any subsequent read command returns the data at the next address in the screen memory. A new dummy read operation is not required until the cursor address is altered by the control program.

When the LC screen is set to graphics mode, all graphics data to be displayed

A11	0	0
A10	0	0
A9	0	0
A8	0	0
A7	0	1

A6 A5 A4	A3 A2 A1 A0	D7 D6 D5 D4 D3 D2 D1 D0	D7 D6 D5 D4 D3 D2 D1 D0
0 0 0	0 0 0 0	1 1 1 1 0 0 0 0	0 1 1 1 0 0 0 0
	0 0 0 1	1 0 0 0 1 0 0 0	1 0 0 0 1 0 0 0
	0 0 1 0	1 0 0 0 1 0 0 0	1 0 0 0 1 0 0 0
	0 0 1 1	1 1 1 1 0 0 0 0	1 0 0 0 1 0 0 0
	0 1 0 0	1 0 1 0 0 0 0 0	1 0 1 0 1 0 0 0
	0 1 0 1	1 0 0 1 0 0 0 0	1 0 0 1 0 0 0 0
	0 1 1 0	1 0 0 0 1 0 0 0	0 1 1 0 1 0 0 0
	0 1 1 1	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0
	1 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0
	1 0 0 1	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0
	1 0 1 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0
	1 0 1 1	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0
	1 1 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0
	1 1 0 1	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0
	1 1 1 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0
	1 1 1 1	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

0 0 1	0 0 0 0	1 1 1 1 0 0 0 0	
	0 0 0 1	0 0 1 0 0 0 0 0	
	0 0 1 0	0 0 1 0 0 0 0 0	
	0 0 1 1	0 0 1 0 0 0 0 0	
	0 1 0 0	0 0 1 0 0	

Fig. 7. Illustrating the compiling of a dot pattern matrix to be loaded into an add-on font EPROM.

corresponds to dot information written into the screen memory. The controller is switched to graphics mode by programming a logic 1 for bit 1 in the mode register. The graphics information can then be written direct to the screen memory. Data can be loaded as separate bytes after loading the start and cursor address, similar to the procedure followed in the text mode. Before sending the

databyte it is, however, necessary to call register 12 via CTRL-WR, and then write the data to DATA-WR. The dot usage of the controller is shown in Fig. 6. The listing of Fig. 9 may also help to analyse the operation of the graphics mode in further detail. Like ASCII characters, dot information can be read back from the display — write 13 to CTRL-WR, then perform a dummy

Table 4

HD61830B Register Overview

Register								Data											
CTL	R/W	RS	D87~D84	D83	D82	D81	D80	Function	R/W	RS	D87	D82	D85	D84	D83	D82	D81	D80	
0	0	1	0	0	0	0	0	Mode control	0	0	0	0	Mode data						
1	0	1	0	0	0	0	1	Vertical/horizontal character pitch	0	0	(Vp - 1) B				0	(HP-1) B			
2	0	0	0	0	0	0	0	Number of characters per line/number of bytes	0	0	0	(LN - 1) B							
3	0	1	0	0	0	0	1	Number of vertical dots	0	0	0	(IN - 1) B							
4	0	1	0	0	1	0	0	Cursor position	0	0	0	0	0	0	(CP - 1) B				
5	0	0	0	0	0	0	0	Display starting address (least significant) (Lower)	0	0	Address data								
6	0	0	0	0	0	0	1	Display starting address (most significant) (Upper)	0	0	0	0	0	Address data					
7	0	1	0	1	0	1	0	Cursor address (least significant)	0	0	Address data								
8	0	1	0	1	0	1	1	Cursor address (most significant) (Upper)	0	0	0	0	0	Address data					
9	0	1	0	1	1	0	0	Refresh memory write	0	0	Character code/bit data								
10	0	1	0	1	1	0	1	Refresh memory read	1	0	Refresh memory data								
11	0	1	0	1	1	1	0	Bit clear	0	0	0	0	0	0	0	(BN) B			
12	0	1	0	1	1	1	1	Bit set	0	0	0	0	0	0	0	(BN) B			
13	—	—	—	—	—	—	—	BUSY signal read	1	1	BF	*	*	*	*	*	*	*	

read, and, finally, read the bit configuration at address DATA-RD.

Adding a character set

As already stated, the controller can use data in an external EPROM to form an additional character set. Figure 7 shows how the controller converts EPROM data into dot patterns on the LC backplane. Using the information given in the figure, a simple computer program may be written to compile a user-defined character table in the EPROM. Alternatively, build the table manually by drawing the character outlines on squared paper. A ready-programmed EPROM with two additional character sets is available as stated in the Parts List.

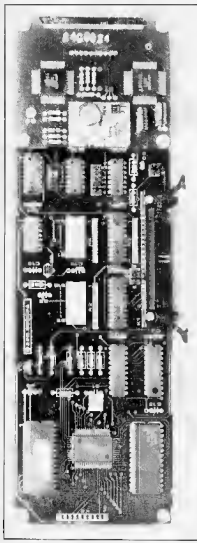


Fig. 8. Completed interface board fitted on to a Sharp LM40001 LC screen module.

```

10 REM          SHARP LM40001G WITH HD61930B CONTROLLER  8*50 CHAR S, 8*8 MATRIX
20 DAWR=OFFFH
30 CTLWR=OFFFH
40 LATCH=OFFFH
50 REM .....
60 DATA 3BH
70 DATA 7FH
80 DATA 49
90 DATA 31
100 DATA 7
110 XBY(LATCH)=B: REM .....
120 REM .....
130 FOR CTL=D TO 4 ..... INITIALIZE HD61930B
140 READ DA: GOSUB 1000
150 NEXT CTL
160 REM .....
170 STARTDR=B: GOSUB 2000
180 REM .....
190 CURADR=D: GOSUB 3000 ..... SET CURSORADDRESS
200 REM .....
210 GOSUB 4000 ..... CLEAR DISPLAY
220 REM .....
230 CURADR=D: GOSUB 3000 ..... SET CURSORADDRESS
240 REM .....
250 CTL=DCH: REM ..... CHARACTER CONTROL
260 FOR X=0 TO 255 ..... WRITE MESSAGE
270 DA=X: GOSUB 1000
280 NEXT X
290 STOP: REM ..... STOP BEFORE GRAPHICS DEMONSTRATION
300 REM ..... ERASE DISPLAY
310 XBY(CTLWR)=0: XBY(DAWR)=32H
320 CURADR=D: GOSUB 3000: STARTDR=D: GOSUB 2000
330 FOR J=0 TO 41: FOR I=0 TO 49: XBY(CTLWR)=12: XBY(DAWR)=0: NEXT: NEXT
340 XBY(CTLWR)=0: XBY(DAWR)=32H
350 REM ..... DRAW PATTERN
360 STARTDR=D: GOSUB 2000
370 FOR L=0 TO 15
380 K=D-3+J
390 FOR I=L TO L+3 STEP 1
400 IF I<0 THEN 520
410 CURADR=I+J+50: A=2*((7-X)+2*((6-X)): GOSUB 800
420 CURADR=CURADR+50: A=2*((7-X)+2*((6-X)): GOSUB 800
430 CURADR=49-I+J+50: A=2*((7-X)+2*((6-X)): GOSUB 800
440 CURADR=CURADR+50: A=2*((7-X)+2*((6-X)): GOSUB 800
450 CURADR=CURADR+50: A=2*((7-X)+2*((6-X)): GOSUB 800
460 CURADR=49-I+(J+1)+K+50: A=2*((7-X)+2*((6-X)): GOSUB 800
470 CURADR=CURADR+50: A=2*((7-X)+2*((6-X)): GOSUB 800
480 CURADR=CURADR+50: A=2*((7-X)+2*((6-X)): GOSUB 800
490 CURADR=CURADR+50: A=2*((7-X)+2*((6-X)): GOSUB 800
500 J=J+2
510 NEXT J
520 K=K+1
530 NEXT I
540 NEXT L
550 REM ..... WRITE LCD IN GRAPHIC MODE
560 FOR M=0 TO 2
570 I=M*21
580 FOR J=16 TO 44 STEP 4
590 FOR L=0 TO 2
600 READ A
610 FOR K=0 TO 3
620 CURADR=I+L+(K+J+50): GOSUB 800
630 NEXT K
640 NEXT L
650 NEXT J
660 NEXT M
680 END: REM ..... END
800 GOSUB 3000: XBY(CTLWR)=12: XBY(DAWR)=A: RETURN
1000 REM ..... WRITE CONTROL AND DATABYTE
1010 XBY(CTLWR)=CTL
1020 XBY(DAWR)=DA
1030 RETURN
2000 REM ..... SET DISPLAY STARTADDRESS
2010 CTL=WH
2020 DA=STARTDR AND OFFH
2030 GOSUB 1000
2040 CTL=WH
2050 DA=STARTDR/256
2060 GOSUB 1000
2070 RETURN
3000 REM ..... SET CURSORADDRESS
3010 CTL=DCH
3020 DA=CURADR AND OFFH
3030 GOSUB 1000
3040 CTL=DCH
3050 DA=CURADR/256
3060 GOSUB 1000
3070 RETURN
4000 REM ..... CLEAR DISPLAY
4010 CTL=DCH
4020 XBY(CTLWR)=CTL
4030 FOR I=0 TO 39H
4040 XBY(DAWR)=20H
4050 NEXT I
4060 RETURN
5000 DATA 15,0,0,15,0,0,15,0,0,15,0,0,15,0,0,15,0,0,15,0,0,255,255,15
5100 DATA 240,255,0,15,0,15,15,0,0,15,0,0,15,0,0,15,0,15,0,15,0,15,240,255,0
5200 DATA 255,255,0,15,0,15,15,0,15,15,0,15,15,0,15,15,0,15,15,0,15,255,255,0

```

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Fig. 9. Graphics demonstration program for the Elektronics BASIC computer plus LC screen interface described here (LM40001). The program halts at line 290 — type CONT to continue the graphics demo. XBY(...) is an output instruction, and ** stands for mathematical squaring.

PITCH CONTROL FOR CD PLAYERS

In general, only professional compact-disc players are provided with a pitch control. Domestic types so equipped are few and far between, and are also pretty expensive. A circuit is described here that makes it possible for a pitch control to be added to most CD players at a fraction of the cost of a professional unit.

Correct operation of a CD player is ensured by a central, crystal-controlled clock operating at 11.2896 MHz. In the block diagram of a typical CD player—see Fig. 1—this clock is contained in the digital filter chip (SAA7220), but the crystal is external to this IC. The clock controls not only the data processing, such as decoding, error correction, and digital-to-analogue conversion, but also the drive motors.

In CD players less sophisticated than the Philips CD960 (used for Fig. 1), a digital filter is not used and the crystal is con-

nected to the XTAL inputs of the decoder chip (here a Type SA7210).

For the present purposes, it is fortunate that all the circuits of a CD player continue to operate correctly if the clock frequency is altered, although the motors will run faster or slower, depending on whether the frequency is increased or reduced. In principle, therefore, it is fairly simple to alter the speed of the disc drive motor, and thus the pitch of the sound output.

According to most manufacturers, the clock frequency should be within $\pm 10\%$

of the nominal value, but trials in a number of CD players have shown that much greater tolerances are permissible. At very large deviations, however, some special functions, such as skip and search, fail to operate correctly. In the proposed circuit, the clock frequency may be varied between 9 MHz and 13 MHz without any detrimental effects on the electronic circuits in the player. Basically, all that is required is to remove (unsolder) the crystal from the appropriate printed-circuit board in the CD player and replace it by the coaxial cable

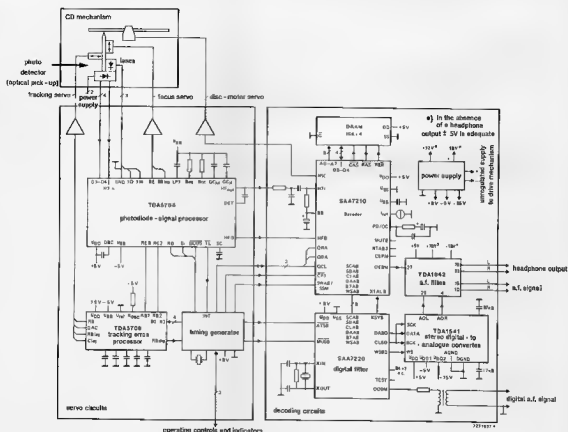


Fig. 1. Block diagram of typical CD player (Philips CD960).

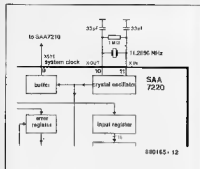


Fig. 2. Detail of the clock oscillator in the digital filter contained in Fig. 1.

from the proposed pitch control. The oscillator circuit of a typical CD player is shown in Fig. 2. It should be noted that replacement of the crystal invalidates the initial manufacturer's warranty.

PLL synthesizer

In professional CD players fitted with pitch control, the variable clock frequency is derived from a simple, free-running voltage-controlled oscillator—VCO—in which the voltage is varied with the aid of a potentiometer, as shown in Fig. 3. When the VCO is in circuit, the frequency, and thus the speed of the disc drive motor, may be altered by turning or sliding the potentiometer. Note that this circuit is provided with a switch that allows instantaneous return

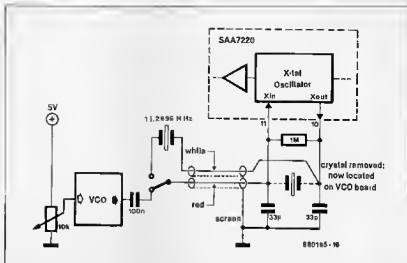


Fig. 3. Many professional CD players use this simple circuit to obtain pitch control.

to the original crystal frequency when required.

This type of circuit has some drawbacks, however: owing to temperature drift, the VCO is not very stable; and the speed variation can not be controlled accurately because of the lack of an indicator. The proposed circuit, therefore, has been enlarged and enhanced as may be seen from its block diagram in Fig. 4 and its circuit diagram in Fig. 5.

The circuit is based on a phase-locked-loop (PLL) synthesizer. The reference

oscillator of the synthesizer is driven by the crystal removed from the CD player. The frequency of the VCO is compared constantly with that of the reference oscillator and made to keep in step with it. This is effected by dividing the reference signal by 400 and the VCO signal by a factor of between 320 and 460. Any deviation of the VCO frequency results in an appropriate correction in the phase comparator. A LED lights when the PLL is not locked. With the PLL locked, operation of the CD player is just as accurate

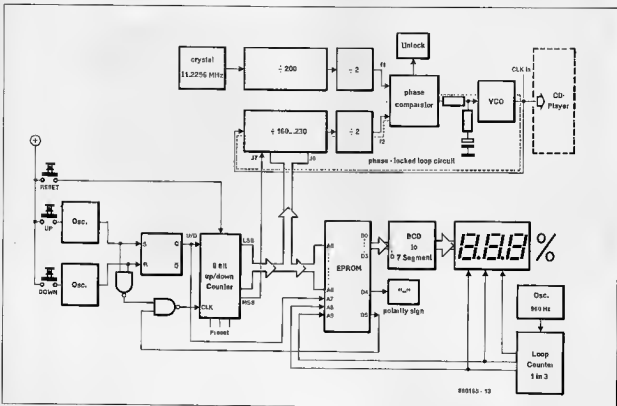


Fig. 4. Block diagram of the pitch control unit.

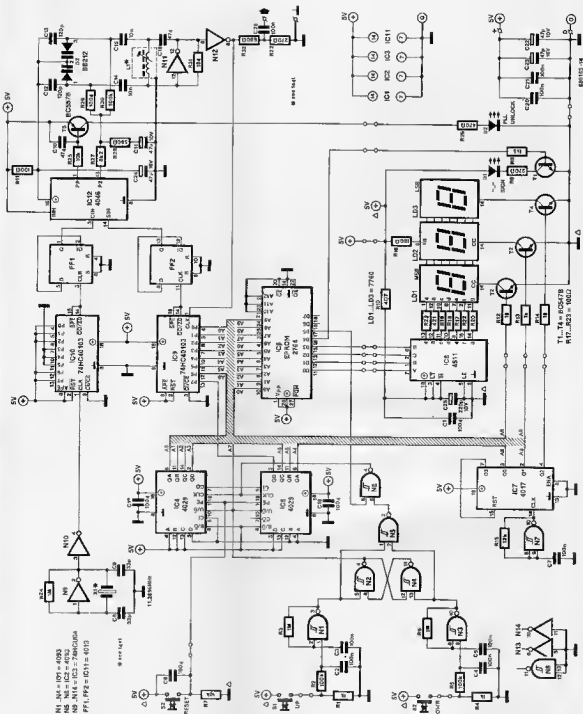


Fig. 5. Circuit diagram of the pitch control unit.

and stable as before the crystal was removed from its original position.

Even when the PLL is not locked, however (indicated by a LED lighting), nothing detrimental happens: the VCO then operates in a free-running mode. The programmable divider in the feedback loop of the VCO is set with the aid of miniature pushbutton switches that control an 8-bit up-down counter. The output data of the counter may vary the divide factor of counter ICs between 160 and 230.

The up-down counter is also connected to EPROM ICs. This circuit is used as a decoder driving a three-digit display. The binary output of the up-down counter is converted into 0.5% steps on the display: 11001000 represents 00.0%. Starting from a counter output of 11001000 (decimal 200), each change of 1 bit (more or less) causes a display shift of 0.5%.

The EPROM also limits the frequency shift to -20% and +15%, because bit 6 (D₆) at its output is fed back to block the up-down counter.

The EPROM also provides polarity indication: when the up-down counter output decreases, diode D₁ lights to show the minus sign.

Since the EPROM content is divided into three, a Type 4017 IC is used for multiplexing the three display segments. Apart from main dividers IC₉ and IC₁₀, there are two bistables in IC₁₁ that serve as binary scaler. These dividers ensure that the phase comparator is provided with true square-wave pulses to prevent any problems in the phase comparison. The circuit of IC₁₂ is shown in Fig. 6. The time constant of network R₁₂-R₁₃-C₁₁ at pin 13 determines the regulating

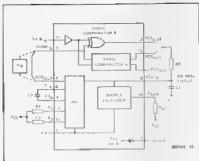


Fig. 6. Internal circuit of phase comparator chip Type 4046.

time of the PLL. The regulating voltage is applied to double variable-capacitance diode D₁ in the VCO circuit.

The frequency of the VCO is determined by L₁-C₁₂-C₁₃-D₁. The oscillator is basically the same as the original crystal oscillator.

The oscillator signal is fed via inverter N₁₂ to the output terminal and also to divider IC₉. The potential divider at the output, R₁₂-R₁₃, provides level matching and forms a low-pass filter with the capacitance of the coaxial cable and the capacitor at the XIN terminal of the SAA7220 in the CD player. Both these measures ensure that the signal at pin 11 of the SAA7220 is a true sine wave at a level of about 1 V_{pp}.

Practical considerations

A phase-locked loop synthesizer on CMOS ICs and operating over the range 9-13 MHz can be constructed properly only on the carefully designed PCB

shown in Fig. 7. It is essential that the supply lines are decoupled properly as, for instance, those to the VCO by R₁₁ and C₁₄.

Since the pitch control circuit draws up to 220 mA, it will normally not be possible to take the power supply from the CD player. A simple +5 V supply will do, however.

Note that because of the high frequencies the dividers in the PLL should be HC or HCT CMOS types; all other ICs may be standard CMOS.

The simple content of the EPROM is given in Fig. 9 to enable constructors to program this device themselves.

Coil L₁ consists of 16 turns enamelled copper wire of 0.2 mm diameter on a Neosid Type 7F1S former. The ends of the winding are soldered to two of the five pins on the base of the former, which themselves are soldered to the PCB.

The inductor is trimmed with the aid of a non-conducting trimming tool. The core is situated correctly if UNLOCK diode D₂ does not light at the extremes of the frequency range (+15% and -20%).

It is best, however, to trim the inductor with the aid of a frequency counter. It is then possible to make the readings on the 3-digit display (in %) and on the counter (in MHz) equal. If the PLL is not locked properly, the reading on the counter becomes unstable and D₂ will light.

With L₁ trimmed correctly, the regulating voltage at pin 13 of the phase comparator must be about 0.5 V at +15% frequency shift, and around 4.0 V at -20%.

It is also possible, if a frequency counter

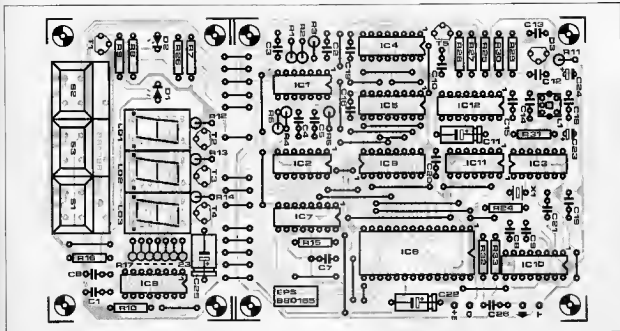


Fig. 7. Printed-circuit board for the pitch control unit.



Fig. 10. Pitch control unit connected to one of the prototypes, a Philips Type CD960 CD player.

It is also possible to alter the frequency of the oscillators driving the up-down counter to some extent. With the UP or DOWN key depressed, the reading on the display increases or decreases in steps. The rate of change of these steps is determined by time constant R_1-C_1 or R_2-C_2 . Increasing the value of either the resistor or capacitor makes the reading change more slowly.

If the supply voltage comes on too slowly, it may be that the value of C_1 is too low for power-on-reset. Either the value of the capacitor or that of R_1 may be increased to speed up the operation (R_1 may be increased up to 100 k).

The PCB in Fig. 7 may be cut into two to give separate synthesizer and display boards. It is then, for instance, possible to fit the display (as in the prototypes) into the CD players behind a small window to make frequent readings possible. It is, of course, also possible to construct the pitch control unit in a self-contained metal case and connect this to the CD player via as short a length of coaxial cable as possible. The case must be earthed to obviate external radiation of the 11 MHz clock signal.

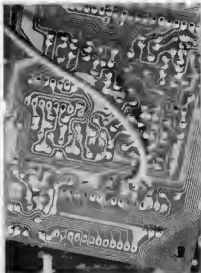


Fig. 11. Connection of the coaxial cable from the pitch control unit to the relevant board in the CD960.

COMPUTER-AIDED TEST EQUIPMENT

by A.W. Moore, MA

The (relatively) low cost, ease of use and flexibility of the personal computer make it eminently suitable for the control of test and measuring instruments. Many instrument and computer makers have realized this and have brought on to the market a number of parallel and serial buses to link a personal computer to one or more suitable instruments.

Not all that long ago, electronic equipment could be tested by the measuring of a few parameters (voltage, frequency, and so on) at some selected points in the circuit. Nowadays, much of such equipment is controlled by a microprocessor. Testing of this kind of equipment can only be carried out effectively by measuring the relevant parameters at many points in the circuit. Moreover, a number of these measurements needs to be taken simultaneously, owing to their interrelation.

With electronic equipment becoming more complex, instruments for testing such equipment have become more complex also and many are now controlled by a microprocessor. Such instruments are called automatic test instruments. If the internal microprocessor is controlled by an external computer, we speak of computer-aided test equipment.

Computer-aided test equipment may be dedicated, i.e., specifically designed and made for the relevant purpose, or it may consist of a PC controlling general-

purpose instruments as shown in Fig. 2. A number of internationally well-known manufacturers, such as Philips, Hewlett-Packard, Tektronix, Schlumberger and Siemens have marketed dedicated computer-aided test equipment, but these are beyond the scope of this article. If several instruments are to be controlled by a single PC, as in Fig. 2., it is an obvious advantage if a common bus is used. Such a bus makes the set-up very flexible since it allows extra instruments to be added without much trouble.

Bus used to link the various items in a test set-up should be of a standard design to enable instruments supplied by different manufacturers to interface. A number of standards has come about as a result of co-operation between various manufacturers, and some of them have been accepted by standards organizations, such as the IEEE and IEC.

There are parallel and serial buses, as well as Local Area Networks (LANs). Some buses are used for intra-board connection, such as the STD (IEEE961) bus, the VME (Versatile Module Europe) bus, and the Futurebus (IEEE896), whereas others are used for interconnecting instruments. Of the latter, the best known is the IEEE488. The IEC625 bus incorporates the IEEE488 standard, but uses a different connector. Local Area Networks are used to connect a variety of different terminals together over a given area.

The parallel intra-instrument buses are fundamentally compatible and are usually called general-purpose interface buses (GPIBs). A GPIB allows up to 14 instruments and a computer to be connected together. The instruments may be listeners (which can only receive data) or talkers (which can only send data).

Many instruments manufactured nowadays are provided with a GPIB interface and switches that are used to set the bus address.

Sixteen active lines are used to implement the GPIB, and these are divided into three groups as shown in Table 1.

The eight data lines are bidirectional and data is transferred byte by byte.

The control bus consists of five lines. When the ATN (attention) line is actuated (by the PC), it signifies to all instruments on the bus that they must give up use of the bus and interpret the data bus as commands. The IFC (interface clear) line is asserted by the PC and used to initialize the instruments. The REN (remote enable) line is used by the PC to instruct the instruments to be ready for remote control. The SRQ (service request) line is used by an instrument to interrupt the controller to signal that it requires attention. The EOI (end or identify) line is used to indicate the end of a multiple-byte transfer or, with ATN, to force the PC to execute a polling sequence.

The transfer control lines control the transfer of data on the data bus. The DAV (data valid) line is set by a talker to indicate that valid data are present on the data lines. The NDAC (not data accepted) line is set by a listener during reading the data. The NRFD (not ready for data) is set by a listener to indicate that not all listeners are ready to accept data.



Fig. 1. Typical computer-cum-instruments set-up.

Table 1

	Pin		Function
Data bus	1	Data line	D ₁
	2		D ₂
	3		D ₃
	4		D ₄
	13		D ₅
	14		D ₆
	15		D ₇
	16		D ₈
Control bus	5	Control line	EOI
	9		IFC
	10		SRQ
	11		ATN
	12	Screen	
	17	Control line	REN
Transfer bus	6	Transfer line	DAV
	7		NRFD
	8		NDAC
	18		
	19	ground	
	20		
	21		
	22		
	23		
	24	Logic ground	

The IEEE488 standard does not define the syntax or code of messages on the bus.

Some typical available equipment

The Intepro Micro Series power supply test equipment from Limerick-based Intepro Systems is a PC expanded with a

bus extender card that is complete with memory and capable of linking up to 255 plug-in instrument modules. Modules currently available include DVM, scanner, power relay, and ripple-and-noise measurement boards.

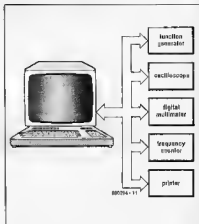


Fig. 2. Typical GPIB structure.

A full range of plug-in data acquisition and controls cards for IBM PCs and compatibles is available from Bleu Chip Technology.

Digital interface cards include the PIO-48 that has 48 programmable input or output lines. Other digital cards have optocouplers, Darlington drivers, relays and counter/timers.

The AIP-24, one of the analogue range, has 24 channels, 12-bit analogue-to-digital converter, sample-and-hold, and a programmable gain amplifier. Other cards include multi-function cards with analogue and digital channels, thermocouple inputs and communications cards with RS232, RS422, RS485, and 20 mA standards.

ANALYSER software from Number One Systems is claimed to have become the largest selling Circuit Analysis software package in Britain with versions for the BBC and IBM (and compatible) PCs.

By simulating accurately the AC performance of a circuit design, it can give the designer confidence that circuits will behave as required, without his needing to resort to expensive test and measuring equipment while "fine tuning" a design. At higher frequencies, unanticipated effects caused by interelectrode capacitances and so on are immediately made clear.

ANALYSER performs an AC Frequency Response analysis on circuits entered into the software, and presents results in tabulated and graphical form. Analysis of gain, phase, group delay, input impedance, and output impedance versus frequency are made to give the electronic circuit designer a powerful tool with which to assess the performance of designs. Particularly useful is the ability to change one or more component values and recalculate to see what the effects of such changes are. This allows rapid solutions to design problems, and minimizes the need for breadboarding and the resultant waste of components and, more important, time.

Strays and parasitics at higher frequencies may also be taken into account. ANALYSER allows resistors, capacitors, inductors, transformers, field-effect and bipolar transistors, operational amplifiers, transmission lines and microwave striplines to be included as circuit elements. Circuits up to 60 nodes and 180 components may be analysed, and there are libraries of active components available that hold the pre-entered specifications of up to 26 of each type (bipolar transistor, FET, opamp). Data may be changed by the user to suit the types most commonly worked with.

Although not strictly a "computer-aided" test equipment, Fieldtech's ORGANIZER II and COMMS LINK are of interest to note.

The ORGANIZER II takes the place of a PC as controller to drive IFR test instruments. Since the unit is little bigger than multi-function calculator, it may be used as hand-held controller that can be stored in the test-set lid when not in use.



Fig. 3. PSION organizer radically changes RS-232 control & storage potential of IFR test instruments.

Some useful addresses.

Amplicon Electronics Ltd
Richmond Road
BRIGHTON BN2 3RL
Telephone (0273) 608331

Blue Chip Technology
Main Avenue
Hawarden Industrial Park
DEESIDE
Clwyd CH5 3PP
Telephone (0244) 520222

Fieldtech Heathrow Ltd
Hamavia House
470 Bath Road
LONGFORD UB7 0LL
Telephone 01-897 6446

Fluke Ltd
Colonial Way
WATFORD WD2 4TT
Telephone (0923) 40511

Hewlett-Packard Ltd
Nine Mile Ride
WOKINGHAM RH11 3LL
Telephone (0334) 773100

Inlepro Systems Ltd
Crescent House
77-79 Churchchurch Road
RINGWOOD BH24 1DH
Telephone (0425) 471421

Keithley Instruments Ltd
1 Boulton Road
READING RG2 0NL
Telephone (0734) 861287

Number One Systems Ltd
Harding Way
Somersham Road

St. Ives
HUNTINGDON PE17 4WR
Telephone (0480) 64778

Philips Instruments
Mallard House
Torrington Place
LONDON WC1E 7HD
Telephone 01-580 6633

Schlumberger Instruments
Victoria Road
FARNBOROUGH GU14 7PW
Telephone (0252) 544433

Siemens Ltd
Siemens House
Windmill Road
SUNBURY-ON-THAMES TW16 7HS
Telephone (09327) 85691

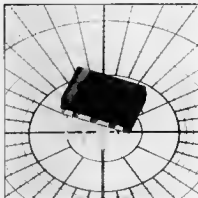
Tektronix Ltd
Fourth Avenue
Globe Park
MARLOW SL7 1YD
Telephone (06284) 6000

BACKGROUND TO E²PROMS

Memory chips with large storage capabilities invariably steal the limelight these days. There are, however, many interesting low-capacity devices available as well. One of these is the electrically erasable programmable read-only memory - E²PROM. Its low cost, versatility and ease of programming make this device an ideal component for many applications involving the permanent storage of, for instance, instrument configuration data.

As an example of the operation and application of a typical E²PROM (or EEPROM), this article discusses the 256-bit Type NMC9306 from National Semiconductor. Readers of this magazine will recognize this device from the *Microcontroller-driven power supply* (Ref. 1), where it is used to for storage and retrieval of voltage and current settings associated with 3 user-selectable instrument configurations.

Basically, an E²PROM couples the non-volatility of an EPROM to the flexibility of a RAM. In this sense, it is functionally similar to a RAM with battery back-up, or a zero-power RAM (e.g. the 48Z02). Among the advantages of the E²PROM discussed here are its low cost and simple-to-use serial interface, which is of particular interest when the device is to be incorporated in existing systems.



Component availability note:

The NMC9306 is available from ElectroMail, P.O. Box 33, Corby, Northants NN17 9EL. Telephone: (0536) 204555. Stock number: 301-656.

of that application, Philips Test Instruments fit a number of their top-grade frequency meters with an E²PROM that holds data corresponding to the temperature response of the central quartz crystal built into a temperature-compensated oven. The temperature coefficient of each quartz crystal intended for use in these instruments is individually recorded as a curve, which is then digitized and loaded into the E²PROM. The microprocessor that controls the instrument measures the temperature of the oven, loads the relevant temperature coefficient from a look-up table, and corrects the central clock frequency to ensure minimum deviation.

Practical use

An essential difference between an E²PROM and other memory chips is

Features and applications

An E²PROM is a read-only memory, and can, in principle, only be read from. Its special internal configuration, however, makes it possible to erase the device electrically, and re-load it, during normal operation. This obviates the need for exposure to ultraviolet light, and the application of a high programming voltage, required for erasing and programming a conventional EPROM. The NMC9306 is fed from a single supply voltage, 5 V, and has an on-chip step-up converter that supplies the programming voltage. Each of the sixteen 16-bit registers can be erased individually. An important difference with respect to a conventional RAM is, however, the time needed for loading (=writing to) a register. In the case of the NMC9306, this programming cycle takes at least 10 ms per register. Also, the number of write operations is limited to about 10,000 per register. The maximum guaranteed data retention period is 10 years, so that data will need to be 'refreshed' at least once during this time, by means of a erase-write cycle.

As already noted, the E²PROM is ideal for quasi-permanent storing of equipment configuration data. As an example

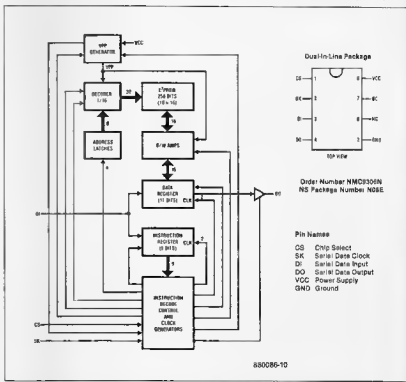


Fig. 1. Block and connection diagrams of E²PROM Type NMC9306.

apparent from the block diagram in Fig. 1. Data is sent to, and read from, the E²PROM via a serial interface, which not only makes it possible to house the chip in an 8-pin DIL package, but also makes its use independent of data- and address-bus structures — the E²PROM is simply a small peripheral device.

The serial input and output pins (DI and DO) may be controlled by separate serial formats. The serial interface is also used for reception, from the host microprocessor, of control commands for the E²PROM. These are 9-bit serial datawords, in which the start bit is always logic high. The next 4 bits form the opcode (see Fig. 2), followed by another 4 bits that form the register address.

The function of the E²PROM control commands can be summarized as follows:

- **Read:** data is first loaded into the data shift-register, and then shifted out via the serial output DO. The shift-out operation is clocked by the low-to-high transition of the signal applied to the SK input. A dummy bit (logic 0) precedes the 16-bit data output string. Only the read instruction causes serial data to be output via the DO line.

- **Erase/write enable (EWEN):** this command should always precede data erasure or loading operations.

- **Erase register:** unlike a RAM, an E²PROM register should be cleared (erased) before loading it with new data.

- **Erase all registers:** similar to the above command, but works on the whole chip rather than on an individual register.

- **Write:** load data in a previously cleared register.

- **Write all registers:** the same data is written to all registers.

- **Erase/write disable:** this command prevents accidental clearing or overwriting of registers.

Instruction	SK	Op Code	Address	Data	Comments
READ	1	00xx	A3A2A1A0		Read register A3A2A1A0
WRITE	1	01xx	A3A2A1A0	D15-D0	Write register A3A2A1A0
ERASE	1	11xx	A3A2A1A0		Erase register A3A2A1A0
EWEN	1	0011	xxxx		Erase/write enable
EWDS	1	0000	xxxx		Erase/write disable
ERAL	1	0010	xxxx		Erase all registers
WRAL	1	0001	xxxx	D15-D0	Write all registers

NOTE: CS=0 enables the 7 instructions as shown. Note that MSB of any given instruction (a 1) and its value as a start bit in the instruction sequence. The next 4 bits carry the op code and the 4-bit address for 1 of 16 16-bit registers.

X is a don't care state

880096-11

Fig. 2. Instruction set of the NMC9306 16x16-bit E²PROM.

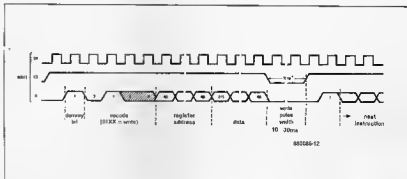


Fig. 3. Timing of the E²PROM write cycle.

Two control lines on the E²PROM arrange the timing. Low-to-high clock transitions on line SK (serial data clock) control the shifting in and out of data and commands. The maximum clock frequency is 250 kHz. Line CS (chip select) is active high, and enables or disables all data and command I/O operations. It also serves to time the erasure and programming pulses, which should have a duration of 10 to 30 ms. After the loading of a clear or write command, the relevant cycle starts when CS goes low. Programming lasts until CS

reverts to logic 1. In the mean time, input SK is disabled. After programming has been completed, CS may remain logic high to enable loading a new command. When CS is made logic low, the E²PROM is switched to the low-power mode. In between commands, the minimum low-time of CS is 1 μ s.

ELECTRONICS NEWS

SUPER TYPEWRITER

An electric typewriter which can work up to a speed of 9,600 bauds per second will be brought out by Hindustan Teleprinter Ltd. HTL's new models, which can work up to 2400 bauds per second, based on the inhouse R & D, has already been approved by DOT.

HTL achieved a record performance in 1987-88, with increased production and the emphasis was on new technology product line, electronics typewriters,

both Roman and bilingual. The company exceeded the target by 50 per cent in electronic teleprinters, by 100 per cent in electronic typewriters and 116 per cent in modems.

INDIAN SOFTWARE ATTRACTS EEC

Ten Indian companies which recently demonstrated their software package to buyers in the European market received about 100 inquiries, according to a report by the India Trade Centre at Brussels.

Indian companies showed their software alongside international giants like the IBM, Unisys and Honeywell. The Indian

companies which were chosen for the exhibition included Ambal Sarabhai Enterprises, CMC, Datamatics Consultants, Hinditorm Computers, ICIM, Radix computers, Tata Consultancy Services, Wipro Information Technology and Blue Star. Most of the Indian companies found they were highly competitive both for products and services.

Meanwhile, another delegation comprising 18 members participated in COMDEX '88, America's biggest trade fair in software, microcomputers and peripherals.

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AUTONOMOUS INPUT/OUTPUT CONTROLLER

A user-configurable I/O controller that gives digital and analogue interfacing power to your computer's RS232 outlet. Fast, simple to build and program, and intelligent enough to deal with up to 64 digital and 12 analogue channels, this microcontroller-driven I/O distribution box should prove invaluable in many applications where a computer runs a small or large-scale automated control job, be it industrial or domestic.

Part 1

The autonomous I/O controller described here is basically a versatile, intelligent, computer peripheral that can be connected in the bus structure proposed for the microcontroller-driven power supply published earlier this year (Ref. 1). Like the power supply, the I/O controller derives its intelligence from a Type 8751 microcontroller from Intel. The control program that resides in this chip has been written exclusively for this project in the *Elektor Electronics* design department.

Applications of the I/O box arise almost automatically when a computer is to communicate with the outside world. These applications range from essentially simple, such as the control of LED matrices, relays or electronic switches, to more sophisticated, interactive, ones including the control of motors, but also alarm, heating and air conditioning systems. The list of applications can be extended even further with PC-controlled battery chargers, light shows and audio distribution equipment. The 8-channel ADC in the system allows analogue values provided by a wide variety of sensors to be captured, stored and processed by the computer.

One button — seventy-six I/O lines

The basic operation of the autonomous I/O controller is best understood after looking at the front panel first (Fig. 1) — not a multitude of switches and other controls on this, just the on/off switch and a push-button labelled **DISABLE OUTPUTS** with an associated LED. There is no need for any other form of local operation, because the unit is controlled entirely by commands sent by the host computer it is connected to. There is nothing to look for at the rear side of the unit either: all that is there is the mains input socket and the 9-way D-socket that links the I/O box to the computer.

Part 2 of this article will detail the actual programming of the I/O controller with the aid of a set of commands similar to those used for the microcontroller-driven power supply. BASIC command **PRINT** (or **LPRINT**) is perfectly adequate for sending these commands via the RS232 port, so that even beginners need not worry about bus interfacing, machine language programs, or the intricacies of the microprocessor inside the host computer. Most computers provide

some sort of printer output redirection facility, so that the use of the RS232 port obviates the need for complex programs to 'talk and listen' to the peripherals connected to the I/O box. There is, of course, a price to be paid for all these benefits, and this is mainly the limited speed of the system. None the less, 9600 baud should be fast enough for any of the applications mentioned earlier, since the minimum pulse duration that can be programmed on a digital output line is about 6 ms.

Three printed circuit boards

Figure 2 shows that the autonomous I/O controller can be expanded to user requirements. The system is in principle composed of 3 types of sub-unit:

- **controller board** — this holds the microcontroller, power supply and the 10-bit analogue-to-digital converter (ADC) with its associated 8-channel input multiplexer;
- **bidirectional digital board** — this is identical to that for the 8052AH-BASIC computer (see Refs. 2 and 3);
- **analogue output board** — this is virtually identical to that for the 8052AH-BASIC computer (see Refs. 2 and 3).

There is a slight difference to note between the autonomous I/O controller and the system discussed in Ref. 3. This difference entails the maximum number of peripheral boards (digital and analogue output). In the autonomous I/O controller, there may be 0, 1, 2, 3 or 4 boards of each type, provided each is allotted a unique address (this will be reverted to in Part 2). It is not allowed to replace, for example, two analogue output boards with two bidirectional I/O boards, or the other way around. Push-button **DISABLE OUTPUTS** provides a toggle function for simultaneously switching on and off all *digital* outputs. The current state of this function is indicated by a LED.

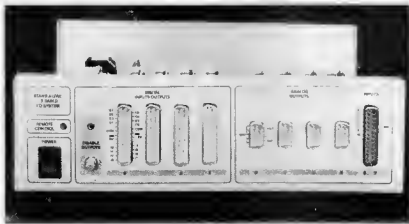


Fig. 1. Front view of the autonomous I/O controller.

An interesting and original feature offered by the system described here is its ability to interconnect pairs of corresponding input and output lines *with the aid of software* (command 'G'). A practical application of this feature is shown in Fig. 5 where a pair of I/O lines is used with manual switch control.

As already noted, the controller board holds the 'brains' of the system, the microcontroller Type 8751, and the ADC with its associated 8-way input multiplexer. The circuit diagram is given in Fig. 3.

Circuit IC₂ is a supply monitor chip that ensures the correct initialization of the microcontroller at power-on. It also works as a watchdog, checking the presence of 1.1 ms long pulses on controller output line P2.0. When these pulses fail, the microcontroller is immediately reset. This is done to prevent the system generating uncontrolled signals when the supply voltage drops below the level needed for correct operation, or when the system 'hangs up' due to some internal malfunction. CPU port line P2.0 is also fed to the bidirectional digital boards. Conflicts with the watchdog are avoided by the microcontroller ensuring that WR is never activated when a pulse is sent to the watchdog chip. Diodes D₁ and D₂ determine the address, or identification code, assigned to the autonomous I/O controller — see Table 1. With 2 diodes, a choice of 4 addresses is available. This will do for most applications, given the large number of lines provided by a single autonomous I/O controller.

accuracy, the reference voltage should be as high as possible, but it must never exceed the supply voltage. The reference voltage is, therefore, set to +5 V, supplied by the well-known precision stabilizer Type REF-02 (IC₅), and the supply voltage to +5.25 V, supplied by an LM317 (IC₆). The voltage difference of 0.25 V is a safety margin that should prevent fluctuations on the output voltage of the LM317 damaging the ADC.

The operation of the serial interface will be discussed in Part 2, as part of the software command descriptions.

- **Modular structure. Largest system configuration supports:**
32 digital outputs;
32 digital inputs;
4 analogue outputs;
8 analogue inputs.
- **Digital interface card has 8 buffered outputs and 8 protected inputs.**
Up to 4 of these modules can be used in I/O system.
- **Analogue output card has 1 output with 10-bit resolution.** Output voltage span: 0 to +10.23 V, programmable in 10 mV steps. Up to 4 of these modules can be used in the I/O system.
- **Analogue-to-digital converter on controller board has 8 multiplexed inputs.** Input voltage span: 0 to +10.23 V. Resolution: 10 mV/LSB.
- **Medium-power open-collector digital outputs are surge-protected, and can handle 50 V; 500 mA loads direct.**
- **Optional internal connection of digital inputs and outputs.**
- **Ideal for multitasking of peripherals on a single serial computer channel.**

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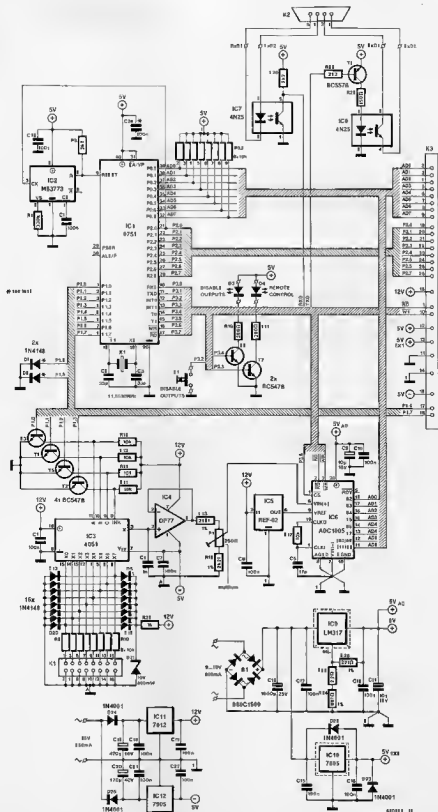


Fig. 3. Circuit diagram of the controller board, which holds the micromicrocontroller, the A-D converter, and a number of peripheral chips.

Analogue-to-digital conversion

The 8 analogue inputs on connector K1 are connected to protective diode-resistor networks. The CPU, IC1, controls the ADC direct, and the input multiplexer, IC2, via 4 level converters, T1 to T3. The INH (inhibit) input of the Type 4051 CMOS analogue multiplexer, in combination with capacitor C4 and opamp IC4, makes it possible to realize a basic sample-and-hold function. C4 is dimensioned such that it provides an acceptable compromise between rise and fall time — the conversion error it introduces is less than 1/2LSB. Potential divider R15-P-R16 scales the sampled analogue voltage down to a value between 0 and 5 V.

The analogue inputs form a high impedance when they are not sampled. When they are, the impedance drops to about 10 k Ω . The procedure for loading and conversion to 8 bits of the 10-bit data in ADC Type ADC1005 is largely similar to that adopted for the Type DAC1006 (for details, see Ref. 3). An important feature of the ADC1005 is its insensitivity to current peaks during the actual conversion process, as well as to occasional negative voltages supplied by opamp IC4. No attempt should be made to suppress the current peaks by fitting a capacitor at the input of the ADC, since this would result in significant conversion errors.

Bidirectional digital card and analogue output card

The circuit diagrams of these modules are given in Figs. 4 and 6 respectively. For a description of the operation, refer to Ref. 3 (but note the value of R2 on the analogue voltage board, and the supply voltages). The address assignment can be deduced from Table 2. The digital I/O cards can only be addressed by fitting jumpers E0 to E3 (on K3), the analogue output boards by fitting jumpers E4 to E7 (also on K3). Do not swap cards of a different type.

Table 2.

K3	Peripheral module
E0	digital card 0
E1	digital card 1
E2	digital card 2
E3	digital card 3
E4	analogue card 0
E5	analogue card 1
E6	analogue card 2
E7	analogue card 3

Construction

The printed circuit boards for building the autonomous I/O controller are shown in Figs. 7 (controller board; double-sided, through-plated), 8 (digital I/O board) and 9 (analogue output board). The 26-way flat-ribbon cable

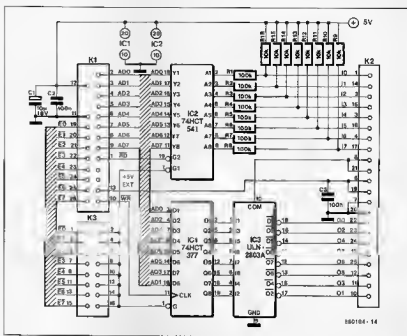


Fig. 4. Circuit diagram of the bidirectional digital I/O card.

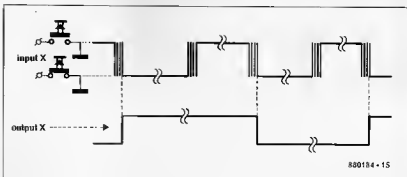


Fig. 5. Key-debounce application of the bidirectional digital card.

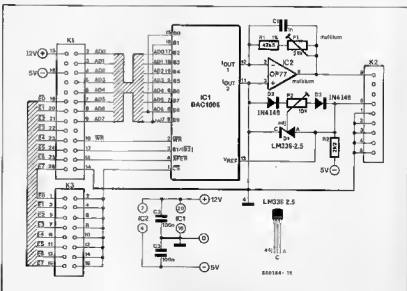


Fig. 6. Circuit diagram of the analogue output card.

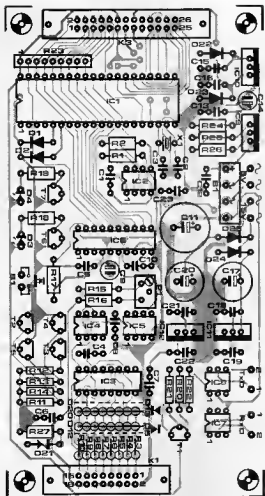


Fig. 7. Component mounting plan of the double-sided, through-plated, controller board of the autonomous I/O controller.

that 'buses' connectors K1 of the digital and analogue boards connects these to the controller board.

Construction of the controller board should not cause difficulty. Note that all electrolytic capacitors are radial types that are fitted upright. Component R23 is an 8-way, 9-pin, single-in-line (SIL) resistor network. Make sure that the protective diodes are fitted the right way around (D1 to D12: cathode up; D13 to D22: cathode down). The 5 V regulators may be fitted on to the cabinet side panel with the aid of insulating washers.

It is recommended to fit supply decoupling capacitor C23 at the track side of the board, straight across pins 20 and 40 of the microcontroller.

The photograph in Fig. 11 shows the prototype of the autonomous I/O controller fitted in an enclosure of the same size as that used for the microcontroller-driven power supply. There is plenty of space left for fitting two mains

transformers (a single type that provides approximately 9 V at 0.8 A, and 15 V at 250 mA, may be difficult to obtain).

The drawing of Fig. 10 and the ready-made, self-adhesive, front-panel available for this project are used as templates for preparing the aluminium front panel of the enclosure. Remember to drill recessed holes for the counter-sunk screws that secure the D-type sockets and anything else attached to the inside of the front panel, such as horizontal support pillars between this and the rear panel. Small additional holes are drilled in the front panel as shown in Fig. 10 to give access the multivolt presets on the analogue output boards (these holes are not provided in the self-adhesive front panel foil, and must be punched after carefully lining up the completed analogue boards behind the aluminium front panel). A sharp hobby knife is used for clearing

Parts list

Autonomous I/O controller Controller board

Resistors ($\pm 5\%$):

R1 = 330K
R2; R20; R21 = 2K2
R3... R14 incl.; R17 = 10K
R15; R16 = 2K21; 1%
R18; R19 = 390R
R22 = 150R
R23 = 10K; 8-way SIL resistor network
R24 = 681R; 1%
R25 = 22R
R26 = 221R; 1%
R27 = 1K0
P1 = 250R multivolt preset (Bourns series 3266, 10p adjustment)

Capacitors:

C1; C6; C7; C8; C12; C13; C14; C16; C18; C19; C21;
C22 = 100n
C2; C3 = 33p
C4 = 1n0
C5 = 47p
C9; C14 = 10 μ ; 16 V; radial
C10 = 100n ceramic
C11 = 1000 μ ; 25 V; radial
C17; C20 = 470 μ ; 40 V; radial

Semiconductors:

B1 = 880C1500
D1; D2; D5... D20 incl. = 1N4148
D3; D4 = LED
D21 = zener diode 10 V; 0.4 W
D22... D25 incl. = 1N4001
T1 = 8C557
T2... T7 incl. = BC547
IC1 = 8751.

IC2 = MB3773 (Fujiitsu)

IC3 = 4051

IC4 = OP-77 (PMI)

IC5 = REF-02 (PMI)

IC6 = ADC1005 (National Semiconductor)

IC7; IC8 = 4N25

IC9 = LM317

IC10 = 7805

IC11 = 7812

IC12 = 7805

Miscellaneous:

K1 = 16-way angled PCB header with spool handles.

K2 = 8-way male sub-D connector (not on PCB).

K3 = 26-way angled PCB header with spool handles.

S1 = miniature push-button.

X1 = quartz crystal 11.0592 MHz (IC Electronics).

PCB Type 880184

the holes for the sub-D connectors in the foil.

Adjustment of the analogue output board is carried out as described in Ref. 3. The board with identification

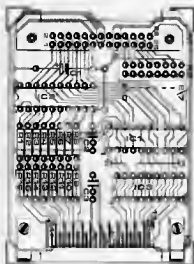


Fig. 8. Printed circuit board for the digital I/O board.

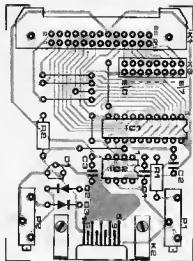


Fig. 9. Printed circuit board for the analogue output board.

Parts list

Autonomous I/O controller:
digital I/O board

Resistors:

R1...R8 incl. = 100K
R9...R16 incl. = 10K

Capacitors:

C1 = 10 μ 16 V
C2; C3 = 100n

Semiconductors:

IC1 = 74HCT377
IC2 = 74HCT541
IC3 = ULN2803A

Other components:

K1 = double-row 26-way right-angled header, or
26-way right-angled male header with eject
handles.

K2 = 25-way D connector, male, with right-
angled pins.

K3 = double-row 16-way straight PCB header.
1 jumper for mounting on K3.
PCB Type BB0153.

Parts list

Autonomous I/O controller:
analogue output board

Resistors:

R1 = 47K Ω 1%
R2 = 2K Ω
P1 = 25K or 22K multiturm preset
P2 = 10K multiturm preset

Capacitors:

C1 = 1nF
C2; C3 = 100n

Semiconductors:

D1 = LM336 2V5
D2; D3 = 1N4148
IC1 = DAC1006 (National Semiconductor)
IC2 = OP-77 (PMI)

Miscellaneous:

K1 = double-row 26-way right-angled header, or
26-way right-angled male header with eject
handles.

K2 = 9-way D connector, male, with right-
angled pins.

K3 = double-row 16-way straight PCB header.
1 jumper for mounting on K3.
PCB Type BB0162



Fig. 10. Front panel drilling template.

number n is programmed to provide 10.00 V with the aid of instruction

$U_n, 10.00$.

The ADC on the controller board is calibrated by applying a precision voltage of 10.00 V and adjusting P_i until the host computer reads exactly this value. Details on programming the autonomous I/O controller will be given in next month's final instalment.

Finally, note that the logic ground and the analogue ground are interconnected at one point only, close to the ADC1005.

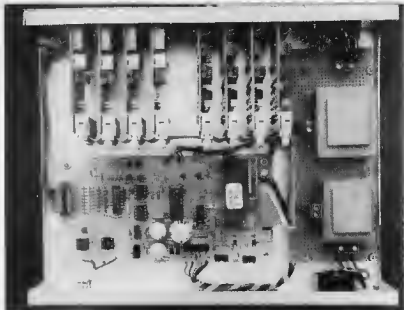


Fig. 11. Internal view of the prototype.

GUIDING THOSE WAVES

by W.D. Higgins

An increasing number of engineers have to consider processing signals in the gigahertz frequency range: satellite TV, information/data systems, point-to-point microwave links, and radar are but a few examples of fields where a basic understanding of the operation of waveguides is required, and where this brief 'guide to waveguides' may prove useful as an introduction.

A waveguide is essentially a precision-engineered length of hollow, usually rectangular, aluminium, invar, copper or brass (70/30 and 90/10) tubing that serves to carry microwave RF signals. Whereas professional-grade coaxial cable is used up to about 3 GHz with considerable attenuation, certain types of waveguide are suitable for carrying RF signals at frequencies of 50 GHz and higher, at an insertion loss that remains negligible even for relatively long runs. Waveguide technology can be treated as a very fine art, but is in principle very similar to conventional plumbing. Since waveguides and ancillaries such as coupling flanges, preformed twists, T-junctions and coaxial transitions are

available ready-made in a variety of sizes, the engineer will have to decide on the most appropriate practical size of the waveguide, bearing in mind cost and machinability. To these factors must be added the technical consideration whether or not a particular waveguide size can be used at the frequency of interest. The physical size of a waveguide determines the lowest frequency at which it can be used, i.e., at which it is capable of propagating RF energy in a relatively loss-free manner. Any type of waveguide, therefore, has its specific cut-off frequency, below which attenuation rises rapidly.

The dominant propagation mode in a waveguide is referred to as TE_{10} . The

distribution of the electric and magnetic field in TE_{10} mode is illustrated in Fig. 1. The electric field strength is maximum at the centre of long walls of the waveguide, and decreases sinusoidally to nought towards the short walls. The magnetic field has a loop-like configuration, and is distributed in parallel with the long wall of the waveguide.

To prevent excessive attenuation, the TE_{10} mode requires a minimum size of the internal waveguide width, w , of 0.5λ . The previously mentioned cut-off frequency therefore corresponds to a wavelength, λ_c , equal to $2w$. Width w should not exceed λ to prevent the dominant mode changing from TE_{10} to another electromagnetic pattern whose

structure causes matching problems at the input and output of the waveguide. In practice, w is made slightly greater than 0.5λ because the wavelength of a signal in a waveguide, λ_g , is greater than the free-space wavelength, λ_0 :

$$\lambda_g = \frac{\lambda_0}{\sqrt{1 - (\lambda_0/2w)^2}}$$

This equation applies to the TE₁₀ mode, and shows that λ_g approaches infinity as w approaches 0.5λ . In practice, the minimum value of w is chosen between 0.6λ and 0.95λ to prevent components or joints in the waveguide causing propagation discontinuities or electrical losses. Similarly, to prevent polarization reversal between the input and output of the waveguide, the internal height, h , is chosen lower than 0.45λ . The maximum frequency of operation of a waveguide is usually $2f_c$.

Standard range

Most manufacturers of precision waveguides produce a standard range of sizes (and materials) that conforms to various European and US specifications. European specifications include IEC153 (I&2), DIN47302, BS9220, DEF5351 (I&2), and CCTU10-20. US specifications include MIL-W-85C, EIA, RS261-A and JAN-MIL.

Waveguide size is denoted by a WG number. The most commonly used sizes are in the range WG5 to WG28 — the higher the WG number, the smaller the waveguide, and the higher the cut-off frequency (remember that this is the *lowest* frequency at which the waveguide can be used). Table 1 gives data of a number of waveguide sizes.

As a rule of thumb, the attenuation of a waveguide increases with length and the WG number. A few examples of typical attenuation figures are included in Table 1. WG16 is particularly popular among radio amateurs for use in 3-cm (X-band) and home-made Ku-band equipment (satellite TV reception). Ex-military waveguide systems are often offered in a variety of configurations at rallies, and by electronic surplus stores. Often, such units come complete with associated SHF electronic parts, such as Gunn-diodes, klystrons, adjustable attenuators, mixer diodes and even horn aerials. Waveguide circulators also exist, but are hard to get hold of.

The usual way of joining lengths of waveguide is by means of flanges. These are slipped over the waveguide and then brazed or soldered in place. Excess waveguide is usually milled or filed away. Great care should be taken to keep the inside of the waveguide free from

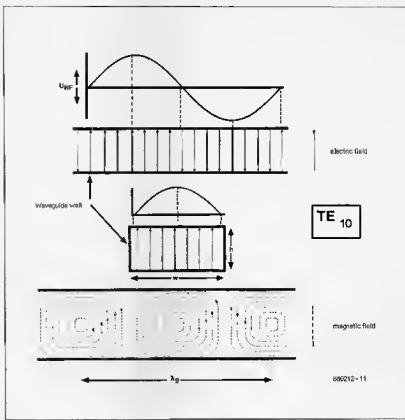


Fig. 1. Relative intensity of the electric and magnetic component in TE₁₀ mode.

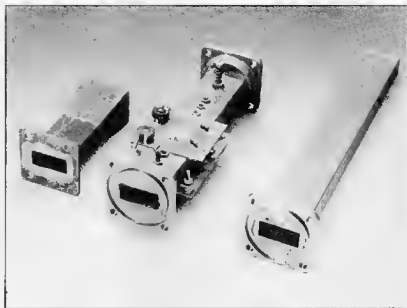


Fig. 4. A piece of WG16 waveguide fitted with one flange, a small horn aerial, and a home-made two-stage Ga-As FET preamplifier for Ku-band satellite TV reception, fitted on to a length of brass waveguide. Input and output coupling to the waveguide is effected with internal $\frac{1}{4}\lambda$ probes.

residual solder, as this introduces high losses. In general, discontinuities smaller than 0.1λ are tolerable, so that it is perfectly possible to make one's own waveguide (and even flanges) from available brass or aluminium tubing. Waveguide tee-pieces, adjustable matching pieces, cross-couplers, dummy loads, tuneable filters, coax adaptors, twists and bends, flexible connecting pieces and directional couplers are available for most types of waveguide. Factors to consider when joining lengths of waveguide, or inserting connectors in a waveguide system, include the frequency range, VSWR of all ports, power division, port-to-port RF isolation, phase balance, power handling, polarization and, of course, physical parameters.

Future trends

As greater use is made of the microwave bands, the demand for waveguides, and with it SHF research and development, is found to increase. In the field of metallurgy, new alloys may be invented with better physical characteristics, to reduce attenuation, improve machinability, and allow greater power handling.

Addresses of companies handling waveguides:

Du-Keren c/o Frequency Techniques •
Cornwallis House • Howard Chase •
Basilston • Essex SS14 3BB. Telephone: (0268) 293401.

Evered • P.O. Box 21 • Lewisham Road • Smethwick • Warley • West Midlands B66 2BW. Telephone: (021 555) 5885.
Flann M.I. • Dunmure Road • Bodmin • Cornwall PL31 2QL. Telephone: (0208) 3161.

Table 1.

WG number	Inside dim. Outside dim. w x h (mm)	Attenuation (dB/m)	Frequency range (GHz)	Cut-off frequency (GHz)	Weight (g/m)	Radio Band
5	195.6 × 97.8		0.96 to 1.46	0.77		
6	165.1 × 82.6	0.00522	1.14 to 1.73	0.91	9.72	L band
7	189.2 × 86.8		1.45 to 2.2	1.16		
8	129.5 × 64.8		1.72 to 2.61	1.37		
9A	86.4 × 43.2		2.2 to 3.3	1.74		
10	90.4 × 47.2		2.6 to 3.95	2.08		S-band
11A	72.2 × 34.0		3.3 to 4.9	2.6		
12	58.2 × 29.1					
12	47.5 × 22.1	0.0355	3.95 to 5.85	3.15	2.18	
13	50.8 × 25.4		4.9 to 7.05	3.71		C-band
14	40.5 × 20.2		5.85 to 8.18	4.3		
15	34.8 × 15.8		7.05 to 10.0	5.3		
	38.1 × 19.1					
	28.8 × 12.6					
	31.8 × 15.9					
16	22.9 × 10.2		8.2 to 12.4	6.6		X-band
17	25.4 × 12.7		10 to 15	2.9		
18	19.1 × 9.5					
18	15.8 × 7.9	0.176	12.4 to 18	9.4	0.48	
19	12.9 × 6.5		15 to 22	11.6		Ku-band
20	10.7 × 4.3		18 to 26.5	14		
	12.7 × 6.4					
21	8.6 × 4.3		22 to 33	17.3		Ka-band
22	7.1 × 3.6		26.5 to 40	21.1		
23	9.1 × 5.6		33 to 50	26.3		
	5.7 × 2.8					
24	4.8 × 2.4	1.06	40 to 60	31.4	0.166	
25	3.8 × 1.9		50 to 75	39.9		mm-band
26	3.1 × 1.6		60 to 90	48.4		
27	2.5 × 1.3		75 to 100	59		
28	2.0 × 1.0		90 to 140	73.8		

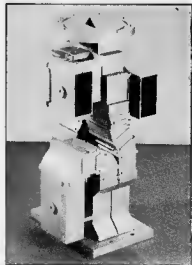


Fig. 2. Not a decapitated robot, this, but a 4-port phase shifter for new high-power C-band radars currently under development in the USA and Sweden. Photograph courtesy of MM Microwave.

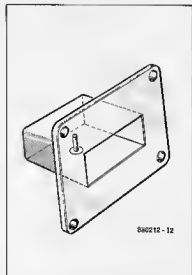


Fig. 3. WG-16 waveguide input of a low-noise block down converter (LNC) for Ku-band satellite TV reception.

LFA-150: A FAST POWER AMPLIFIER (FINAL PART)

from a basic idea by A. Schmeets

Protection circuit. The protection circuit serves to:

- delay the energizing of the output relay by a few seconds from power-on;
- on switch-on, monitor the d.c. resistance of the loudspeaker: if this is lower than 2.2 ohms, the output relay is not energized;
- deactuate the output relay if the direct voltage across the output terminals of the amplifier rises above 1 V; and
- deactuate the output relay if the peak current flowing in the output transistors rises above 10 A;

- deactuate the output relay if one, or both, of the secondary a.c. voltages falls—this also ensures that the loudspeakers are disconnected from the output when the amplifier is switched off.

The circuit diagram of the protection unit is shown in Fig. 9. Note, however, that the output relay and the peak-current detector are located on the current-amplifier board.

The 24-V output relay is actuated by T₄₁ and T₄₃. These transistors form a Schmitt trigger, so that the relay is actuated when the potential across C₄₇ has risen to about 12 V and is de-energized

when that voltage has dropped to about 6 V. The hysteresis is determined by R_{97} and R_{100} .

Inverter T₄₂ in the collector circuit of T₄₁ conducts when the protection circuit is on, and this causes D₂₉ to light.

When the power is switched on, C₄₇ charges via R₃₇. Once the potential across the capacitor has reached a value of about 12 V, T₄₃ begins to conduct. Transistor T₄₃ is then switched on and the output relay is energized.

Capacitor $C_{\alpha 7}$ is shunted by transistor $T_{\alpha 0}$, which enables it to discharge very rapidly if a fault arises. The base circuit of the transistor is connected to a poten-

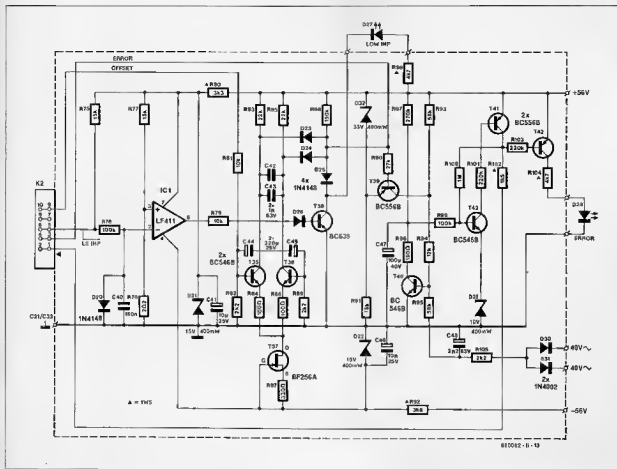


Fig. 9. Circuit diagram of the protection unit.

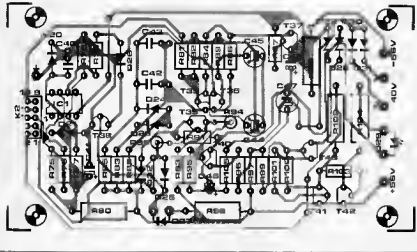


Fig. 10. Printed-circuit board for the protection unit.

Parts list

PROTECTION BOARD

Resistors (±5%):

R75, R77, R81 = 15K
R76, R80 = 100K
R78 = 2R2
R79, R81 = 10K
R80 = 3K3; 1.5 W
R62, R60, R106 = 2K2
R63, R65 = 22K
R64, R66 = 100R
R67 = 330R
R68 = 150K
R80 = 27K
R82 = 3K9; 1.5 W
R83, R85 = 56K
R84 = 12K
R86 = 150R
R87 = 270K
R88, R104 = 4K7; 1.5 W
R100 = 1MΩ
R102 = 1K5; 1.5 W
R103, R105 = 120K

Capacitors:

C40 = 150n
C41, C46 = 10μ; 25 V
C42, C43 = 1μ; 63 V
C44, C45 = 220μ; 25 V
C47 = 100μ; 40 V
C48 = 2μ2; 63 V

Semiconductors:

D20, D23, ..., D28 incl. = 1N4148
D21, D22 = 15 V; 0.4 W zener diode
D27 = yellow or orange LED
D28 = 10 V; 0.4 W zener diode
D29 = red LED
D30, D31 = 1N4002
D32 = 33 V; 0.4 W zener diode
T36, T38, T40, T43 = BC546B
T37 = BF256A
T38 = BC539
T39, T41, T42 = BC556B
IC3 = LF411CN

Miscellaneous:

K2 = 10-way header for PCB mounting
Two IDC sockets to mate with K1 and K2.
PCB Type 8B0092-3

tial divider, R33-R34-R35, which is dimensioned to ensure that the output relay is deactuated as soon as one, or both, of the secondary a.c. voltages fails. The junction R33-R34-C40 is at a negative d.c. potential that is derived from the secondaries of mains transformer Tr. Junction R33-R34 is connected to the base of T38, which with D23 and R33 forms a sort of comparator. Several of the protective measures are controlled via this transistor. When the base potential of the transistor drops below around 23 V (56 V minus the 33-V drop across D23), T38 begins to conduct and the output relay is de-energized.

The value of the d.c. resistance of the loudspeaker is monitored by IC1. The inputs of the circuit are connected to a Wheatstone bridge, one arm of which consists of R33 and the loudspeaker resistance, and the other of R77 and R78. Measurements can, of course, only be effected when the output relay is not actuated, because only then is the voice coil connected to pins 5 and 6 of connector K2 via the relay contacts. Since the d.c. resistance is determined from direct voltages of only a few millivolts, network R33-C40 has been incorporated to prevent error signals arising from ambient noise. Diode D20 limits the potential across C40.

If the d.c. resistance of the loudspeaker drops below the value of R78 (2.2 Ω), IC1 toggles which causes T39 to conduct. Diode D27 then lights to indicate that the loudspeaker resistance is too low. At the same time, the base voltage of T39 is reduced to almost zero via D28: the relay can then not be energized.

When the loudspeaker resistance is higher than 2.2 Ω, the relay is energized a few seconds after power on. The voice coil is then no longer connected to pins 5 and 6 of K2 and IC1 can not monitor its d.c. resistance. A fresh check on the loudspeaker resistance can only be made when the amplifier is switched on again

or another malfunction has caused the relay to be deactuated.

The power supply for IC3 is derived from the ±56-V lines via zener diodes D21 and D22 and series resistors R80 and R81.

The direct voltage at the output of the amplifier is measured by the differential amplifier formed by T35 and T36. The output signal is fed to T35 via potential divider R40-R42, and to T36 via a bipolar electrolytic capacitor formed by C44 and C45. The difference signal across the collectors of the transistors is applied to low-pass section R43-R45-C40. If the d.c. voltage is greater than ±1 V, the collector voltage of either T35 or T36 drops to such an extent that T39 is switched on via D23 or D24 and this causes the relay to be de-energized via T40. The d.c. operating point of the difference amplifier is set with the aid of constant-current source T37. The current is about 2.5 mA.

Transistors T37 and T39 in the current amplifier measure the peak voltage across the emitter resistor of one of the output transistors in the positive and negative half of the output signal respectively. The voltage dividers in the base circuit of T37 and T39 are dimensioned to cause the transistors to conduct when a peak current of 5 A flows through the output transistor. In that case, T37 switches on T39, or T39 switches on T37 in either event, T39 is switched on (via D21 or D22) and de-energizes the output relay, so that the loudspeaker is disconnected.

Power for the protection circuit is taken direct from the ±56 V lines, but power supply monitoring diodes D20 and D21 are connected to the secondary winding of Tr2 (40 V a.c.).

All other connections between the protection circuit and the amplifier are made via connector K2.

The PCB for the protection circuit is shown in Fig. 10. Populating this is not likely to present any problems.

Auxiliary PSU board. This board, shown in Fig. 11, is intended to house the auxiliary transformer, Tr1, rectifiers D35-D38, and smoothing capacitors C34 and C35. The board is designed to be fitted with a number of terminal blocks to facilitate the inter-wiring of the amplifier sections. Make sure that the smoothing capacitors are rated at 100 V.

Construction

The construction details are given for a mono amplifier: two are, of course, needed for a stereo amplifier. The heat sink must be at least 170×80 mm and be drilled in accordance with Fig. 8. Its resistance must be not greater than 0.5 K/W. The holes are made with a 2.5 mm drill and then tapped to receive 3 mm machine screws.

The enclosure used for the prototypes measures 245×120×300 mm; for a stereo amplifier, a larger enclosure is needed. A small section must be cut from its rear panel to make space for the heat sink (see Fig. 1). The heat sink is mounted at a height that allows fitting the AF input sockets underneath it. The mains input and loudspeaker terminals are located beside it.

Mains transformer T_{Tr} , rectifier B_1 , and the ancillary PSU board are mounted on the base panel of the enclosure. The board for the protection circuit may be mounted on top of the voltage amplifier as shown in Fig. 7 or, alternatively, at another convenient place in the case.

The mains on-off switch and the POWER, ERROR and LOW IMPEDANCE diodes are mounted on the front panel.

All components in the current amplifier, except T_{D1} to T_{D4} incl., are fitted at the track side of the board a few millimetres above the surface.

Inductor L_1 consists of 12 turns 1.5 mm thick enamelled copper wire on a hollow former of roughly 15 mm diameter. Resistor R_{D1} is inserted into the centre of the former and the whole assembly is fitted on the board in one go, again a few millimetres above the surface.

Seven solder pins and a 10-way connector are used for the remaining connections with the other sections of the amplifier.

The terminals of T_{D1} , T_{D2} and T_{D3} are bent upwards 90° about 3 mm from their housing. The transistors are then screwed to the heat sink with the aid of insulating washers with the terminals upwards. It should then be possible to fit the current amplifier board on four 10-mm spacers with the transistor terminals protruding through the appropriate holes in the board (see Fig. 5).

Next, the terminals of the output transistors are bent as shown in Fig. 13. These four transistors are then fitted on to the heat sink with the aid of insulating washers and discs, and plenty of heat conducting paste. Take care that the correct washers and discs are used, because the transistors have different cases. The terminals should coincide with the appropriate solder areas on the board. All transistor terminals may now be soldered to the board.

Transistor pairs T_3 - T_4 ; T_5 - T_6 ; T_7 - T_8 ; and T_9 - T_{10} should preferably be matched. If that is not feasible, they should come from the same production batch (normally indicated on their body).

Pairs T_3 - T_4 and T_5 - T_6 are mounted on the board with their smooth sides adjoining. Some heat conducting paste should be applied between each pair, after which the pairs should be tightened together with a nylon cable tie. This is done to ensure that the two transistors in each pair have the same temperature and so prevent their d.c. operating from shifting.

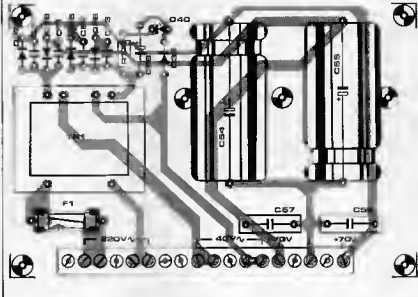


Fig. 11. Printed-circuit board for the ancillary power supply.

The other two pairs are mounted on an L-shaped piece of aluminium, after which the whole assembly (see Fig. 14) is fitted on to the board with the aid of two short spacers. Insulating washers and heat conducting paste should be used in the construction. Solder pins for connections A, B, C, and FB should be fitted at the track side.

When the board is populated, it may be mounted on top of the current amplifier board with the aid of four 35–40 mm spacers.

The mains input plug should preferably be of the type with built-in fuse. From there, a length of mains cable goes to the on-off switch on the front panel. Another length of mains cable goes from the on-off switch to the ancillary PSU board and T_{Tr} .

Make sure that mains-carrying cables and parts are at correct isolating distance from other parts.

The power supply section is wired in accordance with Fig. 12. Note that the secondary (40 V) voltage is applied separately to the ancillary PSU board. The only earth point of the enclosure is wired to the central connection of the 20,000 μ F electrolytic capacitors.

Check whether the two mains transformers are connected in series by switching on the mains and verifying that the voltage at the ± 70 -V terminals is about 70 V with respect to earth. If the voltage is lower, for instance, 45 V, switch off the mains and interchange the two primary connections of T_{Tr} on the ancillary PSU board. Again switch on the mains and check the voltage at the ± 70 -V terminals. When everything is in order, discharge the electrolytic capacitors carefully with the aid of a 470-ohm, 1-watt resistor.

Solder short lengths of (enamelled) cop-

Parts list

ANCILLARY PSU BOARD

Resistor ($\pm 5\%$):

$R_{108} = 1K2$

Capacitors:

C_{50}, \dots, C_{53} incl. = 22n

$C_{54}; C_{55} = 1000\mu; 100 V$

$C_{56}; C_{57} = 680n; 100 V$

$C_{58} = 22\mu; 25 V$

Semiconductors:

D_{35}, \dots, D_{39} incl. = 1N4002

D_{40} = green LED

Miscellaneous:

T_{Tr} = PCB-mount 3 VA mains transformer 2×9

V; 177 mA

F_1 = fuse 50 mA (delayed action); wash PCB

mount holder.

3 off 6 way PCB terminal block.

PCB Type 880092-4 (see

Parts list

MAIN POWER SUPPLY

(not on PCB)

B_1 = BYW68

$C_{51}; C_{52} = 20,000\mu; 63 V$ (or 2×10,000 μ)

F_2 = fuse 2.5 A delayed action.

S_1 = double-pole mains switch.

T_{Tr} = 300 VA toroid mains transformer

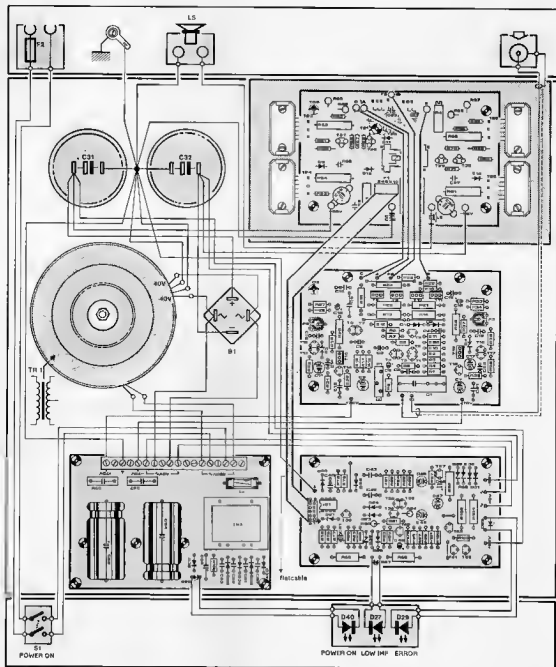
2×40 V; 3.75 A, e.g. ILP Type 73026 (240 V

mains) or 71026 (220 V mains)

Mains input socket with built-in fuseholder.

Heat-sink: thermal resistance $\leq 0.55 K/W$, e.g.

Fischer Type SK47/100-SA (Dau Component).



850292 - R - 18

Fig. 12. Inter-wiring diagram for the various sections of the amplifier.

per wire between points A, B, C, and FB on the voltage amplifier and current amplifier boards.

Connect the input socket to the input of the voltage amplifier by a short length of screened cable.

Connect the power input terminals on the current amplifier board to the take-off points on the electrolytic capacitors by 2 mm thick insulated copper wire. Use similar wire for the connections to the output terminals.

The supply terminals on the voltage amplifier board are connected to the 70-V terminals on the ancillary PSU board. The protection board is connected to the current amplifier board via a length of 10-way flatcable terminated at both ends into a suitable 10-way connector. Make sure that pin 1 of the protection board is connected to pin 1 of the current amplifier board.

Setting up

Set P_1 , P_2 , and P_3 to the centre of their travels, and P_4 to maximum resistance. Switch on the mains supply. After a few seconds, the direct voltages at C_{D1} and C_{D2} should be ± 58 V w.r.t. earth.

Adjust P_2 and P_3 to obtain voltages of ± 60 V across R_{29} and R_{38} respectively.

Adjust P_1 to obtain a direct voltage of exactly 0 V at the junction $L_1-R_{31}-res$.

Adjust P_4 to obtain a voltage of 20 mV across R_{52} and across R_{54} . This voltage indicates a current of around 90 mA through each output transistor, which ensures trouble-free Class A operation.

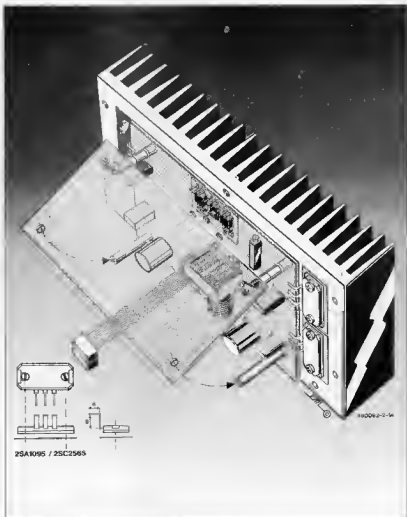


Fig. 13. Mounting of the output and driver transistors on the heat sink.

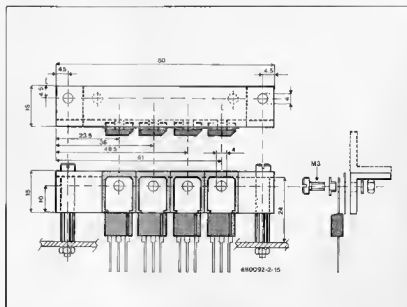
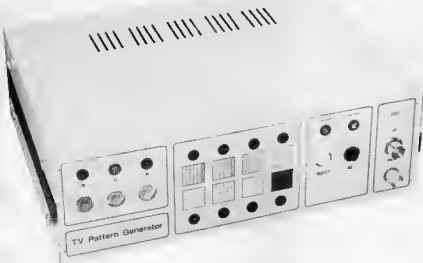


Fig. 14. Construction of the heat sink for T_1 - T_{11} .

COLOUR TEST PATTERN GENERATOR

from an idea by G. Kleine

A PAL-compatible colour video source that supplies a number of test patterns for aligning television sets.



A test pattern generator is virtually indispensable for troubleshooting in television sets because it supplies a video signal that is known to be stable, and thus easily displayed and synchronized on an oscilloscope. Moreover, the instrument allows the user to trace a fault in a TV set or other video equipment by selecting the most appropriate test pattern (e.g. a cross-hatch for convergence testing, or a dot pattern for focusing adjustment).

The test pattern generator discussed here is based on three integrated circuits: a pattern generator (ZNA234E from Ferranti), a video matrix chip with DAC inputs (LM1886) and an associated video modulator (LM1889). The latter two chips are manufactured by National Semiconductor.

Block diagram

The general set-up of the pattern generator is shown in Fig. 1. In principle, all patterns originate from the ZNA234E, which supplies the luminance information for a dot pattern (DOT), a cross-hatch pattern (XH), a horizontal line

pattern and a vertical line pattern. The vertical bar pattern supplied by the chip is not used here because it is unsuitable for generating a colour staircase signal — this is derived from the vertical line pattern.

The output signal supplied by the pattern generator circuitry is monochrome, i.e., it contains only luminance information. Colour is obtained by applying the luminance signal to one or more inputs of the RGB generator. RGB signals are fed via two switches to a colour matrix. The first switch selects between the vertical bar pattern and the other patterns. The second switch disables the colour burst and thus allows the colour staircase to be made monochrome, i.e., to be converted to black, white and intermediary shades of grey. The other patterns can be viewed in black and white also by turning on red, green and blue simultaneously. The monochrome

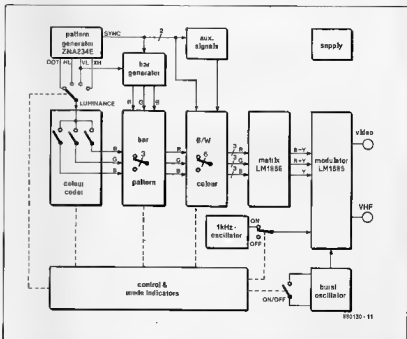


Fig. 1. Block diagram of the test pattern generator.

/colour switch provides the three 3-bit D-A inputs of the colour matrix with an RGB signal whose composition results in 8 colours or 8 shades of grey.

In the colour matrix, the RGB signal is translated into the corresponding levels for the luminance and chrominance component. Colour coding is essentially to the PAL (phase alternation line) standard. The LM1889 combines the signals supplied by the matrix with that of the colour burst generator. The composite video signal thus obtained is available at a buffered output. An RF modulator on board the LM1889 modulates the composite video signal plus a 1 kHz audio test tone on to a carrier in the VHF-I band (approx. 48 to 65 MHz; now no longer used in the UK). An external UHF modulator is required for testing TV sets tuned to channels in the UHF

band. The pattern generator provides a 625-line picture.

Circuit description

The circuit shown in Fig. 2 is not nearly as complex as it looks at first sight. In fact, it is fairly simple, and merely a combination of smaller sub-sections, whose basic function has been discussed above.

Circuit IC₁ provides the pattern signals and two synchronization signals, mixed sync (MS) and mixed video blanking (MVB). The switch that feeds the patterns to the colour generator is formed by IC₄, an 8-to-1 multiplexer. Actually, the circuit referred to as 'colour generator' is composed of three NAND switches, N₆, N₇ and N₁₀. The vertical bar pattern is generated by counter IC₅,

Circuit IC₁₂ is the vertical bar/pattern switch.

The monochrome/colour switch built around IC₃-IC₄ drives the video matrix, IC₁₃, and the modulator, IC₁₄.

The 1 kHz test tone oscillator set up around T₁. This is switched on and off by the logic level at the Q_A output of IC₅ (0 = off; 1 = on). Preset P₁ is adjusted for optimum stability of the oscillator.

The burst oscillator on board the LM1889 operates at the PAL chrominance subcarrier frequency, 4.433 MHz, with the aid of an external quartz crystal and a capacitor network. The user interface of the test pattern generator is formed by push-button switches S₁ to S₆. Each of these controls a function with the aid of a JK bistable (FF₁ to FF₆). Key debouncing is

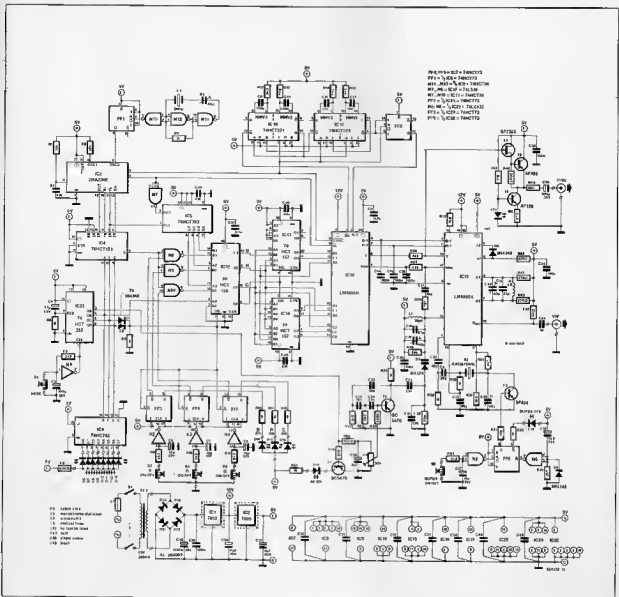
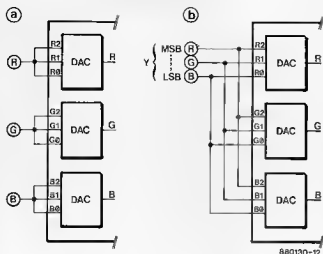


Fig. 2. Circuit diagram of the test pattern generator.



	R	G	B
black	0	0	0
blue	0	0	1
green	0	1	0
red	1	0	0
yellow	1	1	0
magenta	1	0	1
cyan	0	1	1
white	1	1	1

	MSB	+	LSB
black	0	0	0
dark grey	0	0	1
dark grey	0	1	0
dark grey	0	1	1
dark grey	1	0	0
dark grey	1	0	1
light grey	1	1	0
white	1	1	1

Fig. 3. Electronic switches connect the RGB DACs in the EM1886 in two ways: as RGB-TTL inputs (Fig. 3a; colour), or as 3-bit intensity inputs (Fig. 3b; monochrome).

achieved with a combination of a Schmitt-trigger gate (N_2 to N_3) and an R-C network. The logic level at outputs Q and \bar{Q} of each bistable toggles every time the associated key is pressed. LEDs connected to the bistable outputs show the currently selected mode of the pattern generator.

The pattern generated by the circuit is selected by S_2 , whose debounced pulses clock counter IC₃. An auto-repeat function is provided on S_2 . The least significant bit supplied by the counter controls the 1 kHz AF oscillator, so that each pattern is available with or without a test tone. The three most significant counter bits control the pattern selector, the vertical bar/pattern switch, the monochrome/colour switch, and the pattern indicator formed by IC₅ and indicator LEDs D₆ to D₉.

Before the function of the control signals in the circuits is discussed, it is useful to examine the operation of the colour switch.

The simplified diagram of Fig. 3a shows the configuration of the six toggle switches (IC₁ to IC₆) between IC₁₂ and IC₁₄, when 'colour' is selected. Each basic colour has only two shades (satura-

tion minimum or maximum), since the inputs of each DAC are interconnected. For test purposes, this arrangement still results in enough colour combinations.

The switch configuration for 'monochrome' is shown in Fig. 3b. The inputs are connected such that only one 'colour', white, is available, but the intensity can be controlled to give grey and black — the RGB information applied is simply used as a 3-bit luminance (Y) signal.

Returning to the control circuitry of the test pattern generator, D₁, D₂ and R₁ provide an OR function that controls the vertical bar/pattern selector, IC₁₂. A logic high level supplied by D₁-D₂-R₁ selects the RGB signal from gates N_4 to N_6 ; a logic low level, the signal from the vertical bar generator. The fourth switch contact in IC₁₂ controls the monochrome/colour selector. When IC₁₂ is set to 'pattern', IC₁₃ and IC₁₄ are set to the 'colour' position (note that this does not exclude a monochrome picture, since red plus green plus blue gives white). When IC₁₂ is set to 'pattern', the monochrome/colour and colour selection depends on the logic level at the Q₃ output. When this is low, IC₁₃ and IC₁₄

are in the 'colour' position, so that the colour bars are generated. A high level at Q₃ selects the staircase signal for monochrome applications.

As already noted, the bar pattern (monochrome as well as colour) is derived from the signals supplied by IC₁. The pattern is basically generated by the luminance signal for the vertical line pattern, which is composed of a number of pulses at fixed intervals in each line. These pulses are used for clocking a 4-bit counter. Since the three most significant bits function as RGB outputs, the colour obtained changes with every second pulse applied to the clock input. The RGB information remains the same in between two pulses, so that a coloured bar is obtained. Between two lines IC₁₃ is reset by the inverted MVB signal (N_7) to ensure that the counter has the same start state (nought) at each line.

Signals burst enable, $\bar{B}\bar{E}$, H/2, and a bias signal are combined with the available RGB signals in IC₁₁. The chrominance subcarrier generated by IC₁₀ is applied to the bias input, pin 7, of IC₁₁. The other two signals, $\bar{B}\bar{E}$ (burst key) and H/2, are obtained with the aid of monostables MMV₁ to MMV₄, and bistable FF₂. Signal H/2 is the line toggle signal that inverts the R-Y signal for each line in the PAL picture. FF₂ is synchronized by MMV₄ to

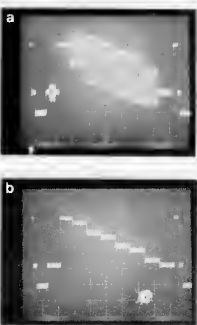


Fig. 4. Oscilloscope photographs showing one picture line in the colour bar pattern (Fig. 4a) and one picture line in the monochrome staircase pattern (Fig. 4b).

ensure that the temporarily doubled horizontal sync-pulse rate in the vertical sync interval does not upset the PAL timing.

The Y-output of IC₁₈ carries a colour CVBS (composite video, blanking, synchronization) signal. The photographs in Fig. 4 show oscillograms of one picture line in the colour bar pattern (Fig. 4a), and one line of the monochrome staircase pattern (Fig. 4b). The CVBS signal is buffered by an amplifier around T₄ to T₆, to enable driving a 75 Ω load.

Unfortunately, the RF modulator contained in the LM1889 can only operate at VHF Band 1 channels (2 to 4). Vestigial sideband suppression is not provided — the RF spectrum generated is simply that of a DSB (double-sideband) modulator. The frequency of oscillation is determined by an external L-C tank circuit, C₁₃-C₁₅-L₁. The modulator is driven with the CVBS signal and the FM sound carrier, whose frequency is set to 6.0 MHz (UK) or 5.5 MHz. Like the chrominance and the RF carrier oscillators, the sound subcarrier oscillator is also contained in IC₁₈. Frequency modulation is achieved with the aid of varicap D₁ which forms part of an external L-C tuned circuit, L₁-C₁₆-C₁₇.

Switching between a colour and monochrome picture is effected by pressing the BURST ON/OFF button (toggle function). The quartz-crystal controlled chrominance subcarrier oscillator is disabled when T₃ conducts.

Construction

The printed circuit board for the test pattern generator, shown in Fig. 5, is a double-sided, but not through-plated, pre-tinned type with a large ground plane at the component side to keep digital interference within limits. All integrated circuits are fitted on to the PCB without IC sockets. In some cases, component terminals (including IC pins) are soldered at both sides of the board to effect through-contacting.

Commence the construction with installing 11 short pieces of through-contacting wire in the vicinity of the boxed EPS number at the component side. Mount and solder one component at a time, and check that pins or terminals, where appropriate, are soldered at both PCB sides. Use a soldering iron with a fine tip.

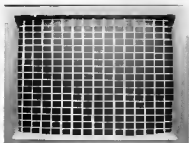
RF inductor L₁ consists of 6 turns of 1 mm dia. (SWG20) enamelled copper wire. The internal diameter is about 6 mm. Space the turns evenly so that the wire ends can enter the holes provided. The photograph of the prototype in Fig. 6 shows that the RF section of the circuit is screened with 20 mm high tin-



Vertical lines.



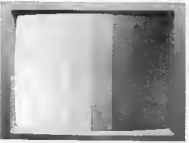
Horizontal lines.



Cross-hatch pattern.



Dots.



Monochrome staircase pattern.

Faultfinding in TV sets

A test-pattern generator is a video signal source intended for locating malfunctions in TV sets and video equipment. Below are a number of possible applications of the instrument described in this article.

Convergence:

Convergence is the intersection, at a specific point at the inside of the multibeam picture tube, of the R (red), G (green) and blue (B) electron beams. Convergence errors are usually observed as beam divergence in the picture corners, where an originally white, single, line diverges in two or more, coloured, lines.

Required test-patterns: cross-hatch or vertical lines.

Focusing:

Focusing and convergence adjustments usually interact, but may use different circuits in the TV set. An improperly focused picture appears blurred and hazy. Like convergence, focusing may have to be optimized with the aid of separate adjustments that work on parts of the screen.

Required test-patterns: dots, cross-hatch and vertical lines.

RGB amplifiers:

Given that the picture tube still has equally active R, G and B emitters, these should have closely matched DC amplification characteristics to prevent colour distortion.

Required test-pattern: colour bar (luminance of individual colours decreases: white, yellow, cyan, green, magenta, red, blue, black).

Uniform saturation on whole screen:

The background colours without a test-pattern enable checking for uniform colour saturation in all areas of the screen. Light spots point to ageing effects in the picture tube.

Burst:

A monochrome picture is generated when the colour burst is turned off. This ability of the pattern generator may be useful for troubleshooting the colour demodulator and chrominance circuits.

Resistors ($\pm 5\%$):

Capacitors:

Notes:

All ceramic capacitors (≤ 1 nF): pitch 5 mm.

All electrolytic capacitors: radial unless otherwise noted.

C1 = 47p
C2: C12; C26; C63... C63 incl. = 47n
C3: C16; C26; C33 = 40p foil trimmer
C4 = 47p, 25 V
C6 = 100p, 25 V
C7; C7; C27 = 10p, 25 V
C9 = 330p
C10; C21; C24 = 22n
C11; C22; C25; C32 = 10n
C13 = 33p
C14; C15 = 100p
C16; C20; C34; C35; C39 = 100n
C17; C30; C31 = 39p
C18 = 27p
C26 = 47p, 25 V
C28; C37; C38 = 47p, 25 V; axial
C36 = 100p, 35 V
C40 = 1000p, 35 V
C41 = 1n0
C42 = 220p

Semiconductors:

D1:D2:D4:D6=1N4148
 D3=BA124 or 88108G
 LEDs...D15 Incl.:D23= LED 5 mm (rectangular)
 LEDs possible for D6 to D13)
 D16= LED; 5 mm; green
 D17= LED; 5 mm; red
 D18= LED; 5 mm; yellow (blue preferred)
 D18...D22 Incl.=1N4001
 T1:T2=BC547
 T3=BF494
 T4:T6=BF199
 T6=8F2668
 I1=7B12
 IC2=7806
 IC3=ZNA234E (Farranti) *
 IC4=74HCT151P
 IC5:IC23=74HCT393P
 IC6=74HCT42P
 IC7:IC9:IC15:IC21:IC22=74HCT73P
 IC9:IC11=74HCT00
 IC10=74LS14
 IC12=74HCT158P
 IC13:IC14=74HCT157P
 IC16:IC17=74HCT221P
 IC18=LM1888N *
 IC19=LM1888N *
 IC20=74LS132

Inductors:

L2 = home-made inductor; see text

Miscellaneous

S1 = double-pole mains switch in mains entrance socket with built-in fuseholder.
S2...S6 incl. = push-to-break button.

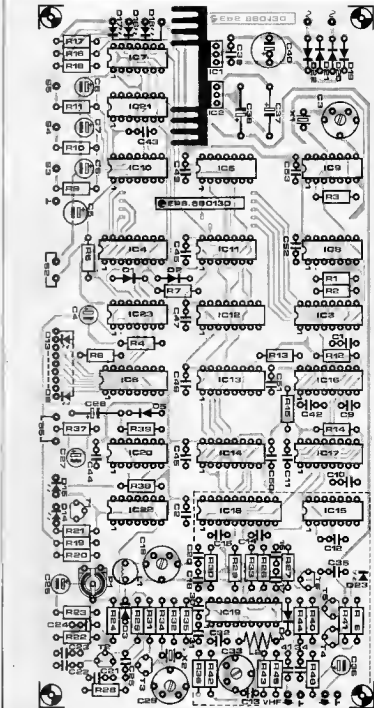


Fig. 5. Component mounting plan of the double-sided printed circuit board.

X1 = 5 MHz quartz crystal in HC18 enclosure.
X2 = 4.433619 MHz quartz crystal in HC1B enclosure.
BNC socket.
Common heat-sink for IC1 and IC2.
Fuse: 100 mA delayed action.
Mains transformer 15 V; 400 mA.
Metal enclosure: approx size 25 x 8 x 18 cm.
TV coax socket.
PCB Type B80130

plate sheets, which are joined in the corners, and soldered on to the ground plane. The screen that runs along IC₁₄, IC₁₇ and IC₁₈-IC₁₅ can only be soldered in the corners and close to C₁₀ because of the tracks running beneath it. Trimmer C₇₀ is to be mounted a few millimetres above the board surface to prevent overheating of the PTFE foil when the two rotor connections are soldered to the ground plane. Finally, on ready-made board 880138, connect pins 1, 2, 3 and 14 of IC₂₂, and pin 1 and 2 of IC₂₁, to ground.

Setting up

The video part of the test pattern generator is fairly simple to adjust. Connect a colour monitor with a 75 Ω CVBS input to the corresponding output of the circuit. Set all trimmers to the centre of their travel, and turn the wiper of P₁ to ground. Press the BURST ON/OFF key when D₁ lights. Carefully adjust trimmer C₅₉ for minimum interference between the coloured bars.

As already noted, the VHF modulator is only for use with a TV set on which VHF Band 1 is available. Tune the TV to, say, channel 3 (in Europe, TV channel E3=55.25 MHz). Adjust C₃ until the test pattern appears. If available on the TV set, use the

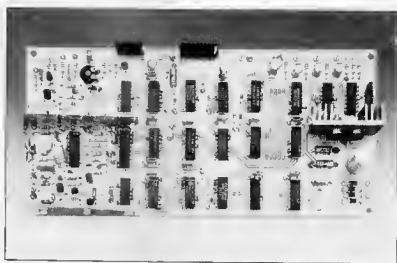


Fig. 6. The completed board (prototype). Note the screening around the RF sections.

fine adjustment to obtain a clear picture; otherwise, carefully adjust C₃ with an insulated trimming tool. Turn up the volume on the set and adjust C₁₉ for minimum AF noise. This tunes the sound oscillator to the correct subcarrier frequency (6.0 MHz or 5.5 MHz, depending on the country you live in). Press S; if D₁₄ does not light. Carefully advance P₁ until the test tone is heard in the receiver. Increase the frequency and

the volume by turning P₁ up to a point where the tone becomes unsteady. Turn the wiper back until the steady tone is restored at maximum volume.

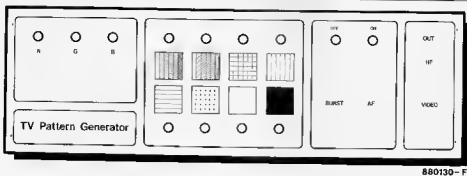


Fig. 7. Suggested front panel layout.

VIDEO & TV: WHICH IS BETTER?

Continued from page No. 1-18

aged. All these 50 to 70 systems could be looked after by one or two motivated unemployed educated youth who could be paid a good salary of Rs. 2,000 per month and motorbike. The same person could also be responsible to handle the software cassettes and circulating them among the villages. A library of 1,000 video cassettes in local language will cost only Rs. 75,000 without any government concession. The ET & T is already selling the 45-minute cassette for Rs. 75. A proper rationalisation of the ex-

cise and Customs duty could enable the distribution of cassettes for still lower prices. The cost of running such a programme for 25 villages over a period of two years will not exceed Rs. 10 lakhs. Of this, 80 per cent of the investment is by way of capital cost. The real cost including depreciation will be a mere Rs. 5 lakhs in two years or Rs. 2.5 lakhs a year. This means the cost per village per year will be Rs. 10,000. For this price, each village will get three complete community video systems, each consisting of 20-inch colour TV and a video player.

There is salvation even for villages without power. The ET & T has developed a very low cost DC battery-to-main converter which could run the combination VCP-TV. A community video set can be operated with a 12 V car battery. Two methods of charging this battery has also been developed. One of these is a system involving stationary bicycle kind of arrangement which drives the dynamo charging the battery. The cost is not more than Rs. 2,000. The other solution is charging through solar panels. In this system, the battery can be charged for the entire year

COMPOSITE - TO - TTL ADAPTOR FOR MONOCHROME MONITORS

Among the welcome side-effects of the current invasion of IBM PCs and compatibles are the drastic price cuts for high-resolution, 12 and 14 inch, TTL-compatible monochrome monitors. The circuit described here makes it possible to use such a display in conjunction with a computer that has a composite video output only.

Many owners of popular home computers must at some time have been envious of IBM PC users, because these are in a position to look at text and graphics on a restive, high-resolution, non-glare monitor instead of on a (modified) TV set tuned to channel 36, and barely capable of displaying 80 characters per line. Until recently, however, the cost of a TTL monitor was such that manufacturers of home computers in the lower price ranges did not even consider equipping these with a digital output. The inexpensive adaptor circuit described here should allow many owners of the first generation of home computers to benefit from the advantages offered by the TTL-compatible monitor.

Circuit description

The circuit shown in Fig. 1 effectively splits the CVBS (composite video-blanking-synchronisation) signal applied to the input into three components: horizontal and vertical synchronization pulses, and video. These three signals are then converted to digital level to enable driving the corresponding inputs on the TTL monitor.

The low reference level of the CVBS signal is first set to 0 V by an active clamping circuit around IC₁. Figure 2 shows the voltage levels in a CVBS signal. Note that the amplitude of U_{sync} is usually about one third of that of U_{video} . The switching threshold of comparator IC₂ is set such that only the synchronization pulses can cause the opamp output to go low. The composite sync signal is then fed to XOR gate N₁ and to a two-section R-L-C low-pass filter. Switch S₁ connected to pin 2 of N₁ selects the signal polarity at the H-sync output. The presence there of V-sync pulses has no consequence for the TTL monitor. The V-sync pulses obtained after filtering in the low-pass are inverted, if necessary, by closing S₂. Inversion is probably not necessary for most types of monitor, but users are well advised to consult the relevant manual in case of doubt.

A fast comparator, based around opamp Type 733 (IC₃) and FETs T₁-T₂, extracts the video component from the CVBS input signal. It should be noted that the attainable contrast ratio is mainly determined by the speed of the opamp, so that the circuit does not work correctly if IC₃ is replaced by a slower type. The toggle point of IC₃ is set to the average video level by P₂. Impedance conversion between the opamp and the digital video input of the monitor is achieved with T₄ and T₅, the latter functioning as an adjustable zener diode.

Construction, setting up and application

The adaptor is constructed on the printed circuit board shown in Fig. 3. The two inductors are preferably ferrite-

encapsulated radial types from Toko. The completed unit can be installed in the monitor, which usually has room to spare inside. This has the advantage that the adaptor can be fed from the existing power supply, ensuring correct interface levels (check the specification of the monitor in this respect). As shown in the circuit diagram, the adaptor is uncritical of the supply voltage level, as long as this is between 5 and 12 V, and well regulated.

An oscilloscope enables the unit to be aligned quickly. With reference to Figs. 2 and 3, measure the levels $\frac{1}{2}U_{sync}$ (x), and $U_{sync} + \frac{1}{2}U_{video}$ (y), and set these voltages as the toggle levels for IC₂ (P₁) and IC₃ (P₂) respectively. Adjust P₂ for optimum picture resolution and stability. When an oscilloscope is not available, set P₂ and P₃ to the centre of

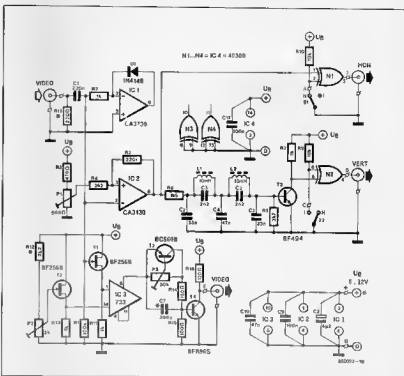


Fig. 1. Circuit diagram of the composite-to-TTL converter.

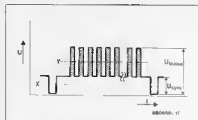


Fig. 2. Toggle level for the sync comparator (X) and for the video comparator (Y).

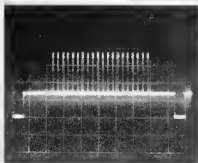
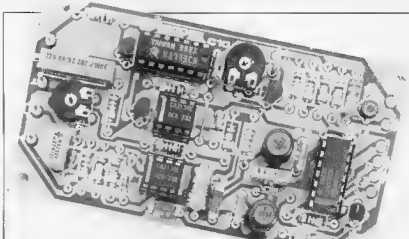


Fig. 3. Oscilloscope display of one line of text in a monochrome CVBS signal supplied by a BBC model B computer.

their travel, and turn the wiper of P_1 to ground. Apply the input signal, and carefully advance P_1 until the picture synchronizes. Then adjust the other two presets for optimum picture quality, first P_2 and then P_3 .

The circuit is dimensioned to work with input video levels between $1 V_{pp}$ and $4 V_{pp}$. The value of R_{17} may have to be increased, or the resistor may have to be omitted, to ensure correct operation with home computers whose output level is lower than $1 V_{pp}$. Signal levels exceeding $4 V_{pp}$ can be accommodated by lowering the value of R_{17} . Capacitor C_7 , finally, also allows some experimenting because it may not be required unless a very high resolution monitor (>80 characters per line) is being used.



Populated printed circuit board.

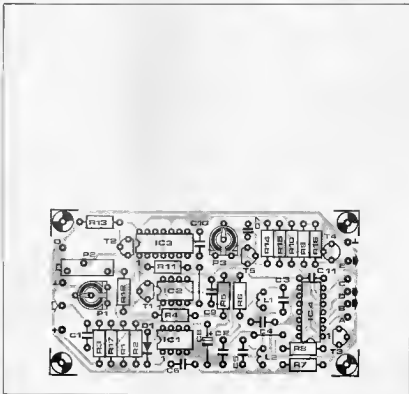


Fig. 4. Printed circuit board for the adaptor.

Parts list

Resistors ($\pm 5\%$):

$R_1 = 100K$
 $R_2, R_6, R_{11}, R_{13} = 1K\Omega$
 $R_3 = 470R$
 $R_4, R_{12} = 2K\Omega$
 $R_5 = 220K$
 $R_6 = 1K\Omega$
 $R_7 = 2K\Omega$
 $R_9, R_{10} = 10K$
 $R_{14}, R_{15} = 100R$
 $R_{16} = 120R$
 $R_{17} = 220R$
 $P_1 = 500R$ preset H
 $P_2 = 2K$ or $2K\Omega$ multiturn preset
 $P_3 = 50K$ preset H

Capacitors:

$C_1 = 220n$
 $C_2, C_6 = 33n$
 $C_3, C_8 = 2n2$
 $C_4, C_{10} = 47n$
 $C_7 = 390p$
 $C_9 = 4\mu 7, 16 V$
 $C_5, C_{11} = 100n$

Semiconductors:

$D_1 = 1N4148$
 $T_1, T_2 = 8F256B$
 $T_3 = 8F494$
 $T_4 = 8F96S$ (listed by Borex Ltd.)
 $T_5 = BC560B$

$IC_1, IC_2 = CA3130$

$IC_3 = \mu A733$ or LM733

$IC_4 = CD4030B$

Miscellaneous:

$L_1, L_2 = 10mH$ radial inductor, e.g. Toko Type 181LY-103 (Circuit stock no. 34-10302).
 $S_1, S_2 =$ miniature SPST switch.
PCB Type 8800098

LOOKING BACK

Updates, applications and improvements for recently published projects

Stereo limiter

(Elektor India, February 1988, p. 2.41.

The operation of this design can be improved with a few minor alterations, which have to do mainly with the DC bias of the gain cells in IC₃. To begin with, C₃ and C₁₀ are replaced by wire links. This upsets the DC bias of A₅ and A₆, however, so that further modifications are required. The positive (non-inverting) inputs are taken to pin 6 and pin 10 of IC₃ instead of to ground. Further, R-C networks are fitted across R₅ and R₁₁ to reduce the direct voltage gain to about unity. The R-C networks only provide negative feedback for direct voltage, and do not, therefore, affect the AC gain. The last modification entails connecting an electrolytic capacitor in series with R₅ (R₁₁). The modified circuit diagram of the stereo limiter is given in Fig. 1.

On the printed circuit board, replace C₃ and C₁₀ by wire links. The R-C networks are soldered direct across R₅ and R₁₁. Remove IC₂ from its socket and bend up pins 3 and 5 before re-inserting the chip. Use short lengths of insulated wire to connect pins 3 and 5 with the indicated pins of IC₃.

HF operation of fluorescent tubes

(Elektor India, July 1988, p. 7.41.

Control of more than one tube.

As stated in the article, the controller is, in principle, suitable for powering one tube only. When two tubes are connected in parallel, a problem arises during starting. Normally, when one tube is connected, resonance will occur at some point when the VCO frequency swings from 80 kHz to 30 kHz, and it is at this point that the tube is started. With two tubes in parallel, one will always start first, causing damping of the resonance circuit and making it impossible for the other to start. Simultaneous starting of the tubes is possible, but a matter of pure chance. Moreover, the current control

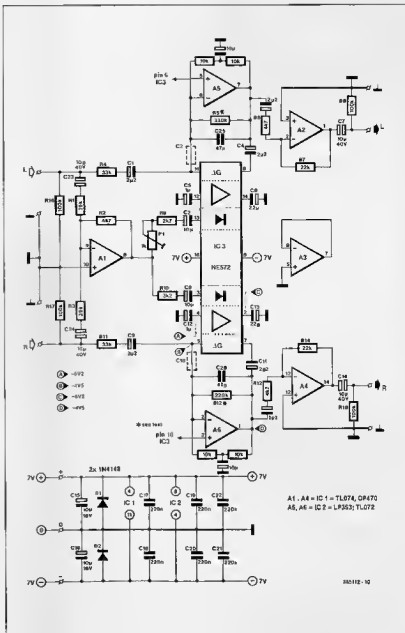


Fig. 1. Modified circuit diagram of the stereo limiter.

circuit and power output stage of the tube controller are not capable of handling double the current.

Series connection of fluorescent tubes offers better perspectives, but works only with relatively low-power tubes of up to 2×20 W. The connection diagram is shown in Fig. 2. Capacitor C_1 is omitted from the board, and 'split up' in C_{1a} and C_{1b} . During starting, C_{1a} and C_{1b} ensure a current flow through all tube filaments, and at the same time provide equal distribution of the start voltage. Since C_{1a} and C_{1b} are connected in series, their value should be double that of C_1 (see Table 1 in the article) to give the correct equivalent capacitance. Two series-connected fluorescent tubes of 20 W each are now equivalent to a single 40 W tube.

Following the simultaneous ignition of the tubes, these can be dimmed as if they were one tube. It will be noted, however, that the point of minimum brightness (set with P_1) is slightly less favourable than with one tube. This is so because at a certain point one tube will go out, but its parallel capacitor will tend to keep the other on. This effect can be explained by the highly irregular impedance characteristic of the fluorescent tube, which behaves like a current-dependent resistance. Series connection of fluorescent tubes is best done with types of the same manufacturer, wattage and age.

There is no way to go round building the required number of HF controller boards when connecting, for instance, two tubes of more than 30 W, or 4 tubes of 20 W. Fortunately, these can still be dimmed simultaneously with a central control as shown in Fig. 3. In this set-up, it is important that the mains connections to the controller boards are in phase.

Cable length between controller and tube.

A cable of several metres length is, in principle, no problem as long as its capacitance is low relative to that of C_1 . In practice, this means that cables from K_1 should not be allowed to run too close to those from K_2 . It is still strongly recommended to fit the controller board as close as possible to the tube, with adequate ventilation, because the use of a relatively high switching frequency on a long cable is bound to introduce a strong electromagnetic field which causes radio and TV interference. The use of shielded wire, however, is not recommended because it increases the capacitance to ground.

Oscillator stability.

The bias current of zener diode D_{12} in the control circuit is relatively low to reduce the current consumption of the control circuit. In some cases, the bias current is too low, however, and gives rise to instability of the zener voltage. This results in temperature dependence of the

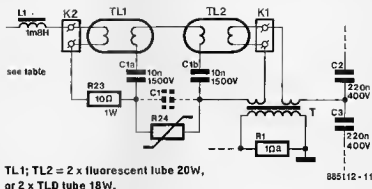


Fig. 2. One controller board connected to two fluorescent tubes.

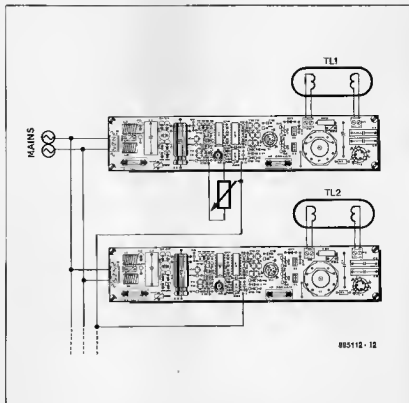


Fig. 3. Showing how controller boards can share the intensity control potentiometer.

oscillator start frequency. To ensure reliable start behaviour of the circuit, it is recommended to redimension a number of components:

R_{16} is changed from 6K8 to 2K7;
 R_{17} is changed from 39K to 15K;
 C_7 is changed from 100 μ F to 220 μ F.

A timer/controller for aquarium lighting is currently under development.

LOGIC FAMILIES COMPARED

by Pete Chown

A brief look at the most important characteristics of recently introduced logic families, and the way in which they can be interfaced to one another.

Today, there exists a bewildering variety of logic families, and the rate at which new families are introduced and older ones become obsolete is perplexing to many. Metal-gate CMOS and standard 74 series TTL are now reaching the end of their useful life. Low power Schottky (LS) TTL is often still the first choice, although this family is now being superseded by HC-MOS. The continued use of LS and S (high-speed) TTL probably results from lack of information about the alternatives. It is not enough to say that LS TTL does the job, however, because alternatives offer reduced power consumption.

The reason for the existence of so many different types of logic integrated circuit is that there is always a trade-off between speed and power consumption. The graph in Fig. 1 shows speed plotted against power. The modern logic families are those nearest to the bottom left, the point which would represent the ideal logic device, offering instantaneous operation at a power consumption of nought. The devices shown in the graph tends to form a line moving between the axes, showing different trade-offs between speed and power. The older devices, LS, 74, 4000 and S, appear above this line. Among the new families is ALS-TTL, Advanced Low-power Schottky, offering devices which are faster and more economical as regards power consumption than pure LS-TTL versions.

High-speed CMOS

The new 74HC and 74HCT series of silicon-gate CMOS devices offer speeds equivalent to LS-TTL, but with negligible power consumption. The 74HC device is the most useful, as it consumes least power, and offers the best range of output voltages for driving external devices (maximum output low voltage $V_{OL}=0.1$ V; maximum output high voltage $V_{OH}=4.9$ V). The problem comes with their inputs. It is here that HC and HCT devices are different. Although +2.4 V might seem a strange value to mean logic high, standard 74 series TTL can give exactly that in the worst case. This level is, however, outside

the specifications for HC devices. IC Manufacturers have been aware of this, and have developed HCT devices by changing the inputs of HC types, so that the worst-case TTL logic high level will be accepted. Full compatibility of HCT with LS-TTL is thus achieved at the cost of a small increase in the power consumption.

HC and HCT devices are excellent for applications where low power and high noise immunity are important design considerations. The quiescent current consumption of an HC-MOS gate is about $0.0025 \mu\text{W}$, increasing to about $170 \mu\text{W}$ at 100 kHz . Silicon-gate CMOS is the superior family when a high fan-out is required, since one output can drive about 1000 inputs. Many devices in the 74 LS-TTL family can practically be replaced by corresponding HCT devices as pin-compatible replacements. It is easy to become over-excited about

the very fast devices, although these will probably have far more impact on us in years to come, probably becoming what LS-TTL is today. We can, however, look forward to getting rid of noisy fans, and to lifting the lid of our PC without the usual blast of hot air.

There are two device families that fall between the ones discussed. These are the 74AS/74ALS series and the FAST[®] series. These two families are really rivals from different manufacturers — ALS is made by Texas Instruments, and FAST[®] by Fairchild and Motorola. The 74AS and 74ALS series offer a substantial reduction in power consumption over the 74S and 74LS series respectively. The fan-out is doubled, propagation delays have been considerably reduced, and the maximum bistable frequency has been increased to 200 MHz.

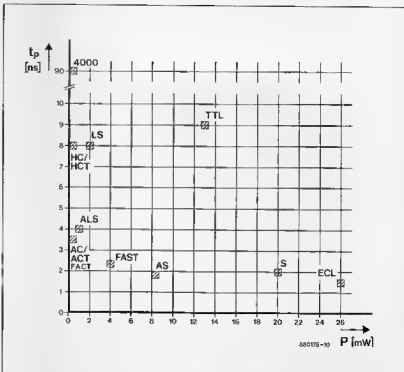


Fig. 1. Speed-power relationships of a number of commonly used logic families.

Interfacing logic families

One of the reasons that designers have been reluctant to use the new logic families is that they are worried about interfacing these devices to existing circuits. The rules for interfacing are quite simple. Many devices are designed to be compatible without any external device. Most others simply need a resistor. The overview in Table 1 gives information on interfacing a number of logic families. The actual value of the pull-up resistor (when required) is chosen to lie roughly between the low value and the high value, which are calculated as follows:

$$R_{low} = \frac{V_{CC} - V_{OL(max)}}{I_{OL} + nI_{IL}} [\Omega]$$

where

V_{CC} = supply voltage;
 $V_{OL(max)}$ = maximum output low voltage;
 I_{OL} = maximum sink current of driving device;
 n = number of device inputs being driven;
 I_{IL} = input current to driven device when input is low.

$$R_{high} = \frac{V_{CC} - V_{IH(min)}}{nI_{IH} - I_{OH}} [\Omega]$$

where

$V_{IH(min)}$ = minimum input high voltage;
 I_{IH} = input high current;
 I_{OH} = output high current.

It will be found that NMOS does not normally need a resistor because this would have a very high value. Not surprisingly, therefore, circuits work well without one. Table 2 lists some commonly used logic families and their parameters, allowing resistance values to be worked out. The resistor should obviously be inserted pulling up to V_{CC} . To choose the correct values to use in the above formulae, take the output parameters for the driving gate, and the input parameters for the driven gate.

Conclusion

If you think the logic market is complex now, it will be even more so in a few years' time, because gallium-arsenide (Ga-As) devices promise operating speeds of around 4 GHz. These new devices will be around in parallel with FACT (Fairchild Advanced CMOS Logic) and existing TTL for a good time, because they will initially be so expensive. The ACT family, like HCT, is fully LS-TTL compatible, while AC gives basically the same drive problems as HC. Both new series are typically 2 to 3 times faster than LS-TTL or HCMOS. It should be noted that AC and ACT

Table 1. Interfacing guidelines

V_{CC} (V_{DD}) of driving and driven device is assumed equal.

Any two bipolar families:	should be compatible
HC to any bipolar:	should be compatible
Bipolar to HC:	pull-up required*
HCT to bipolar:	should be compatible
Bipolar to HCT:	should be compatible
HCT to NMOS:	should be compatible
NMOS to HCT:	normally compatible, but should be checked.

*Calculate value of pull-up resistor from formulae in text.

Table 2.

Parameter	74	74HC	74LS	74AS	74ALS	Unit
$V_{IH(min)}$	2.0	3.5	2.0	2.0	2.0	V
$V_{IL(max)}$	0.8	1.0	0.8	0.8	0.8	V
$V_{OH(min)}$	2.4	4.9	2.7	2.7	2.7	V
$V_{OL(max)}$	0.4	0.1	0.4	0.4	0.4	V
$I_{DH(max)}$	40	1	20	200	20	μ A
$I_{IL(max)}$	-1.6	-0.001*	-0.4	-2	-0.1	mA
$I_{OH(max)}$	-0.4	-4	-0.4	-2	-0.4	mA
$I_{OL(max)}$	16	4	8	20	4	mA

devices have a different supply pinning than LS-TTL, while the number of logic functions currently available is limited to certain bus drivers, and encoders/

decoders. The range of AC/ACT devices is expected to extend considerably, however, in the next year or so.



Good documentation is essential for anyone designing, analyzing and testing circuits based on devices from the new logic families.

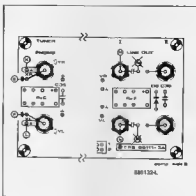
CORRECTIONS

Preamplifier for purists

November 1988 p. 11-37

In the top drawing of Fig. 4, the 47 pF capacitor across R_{31} should be labelled C_{25} , not C_{24} . In the lower drawing, the 47K5 resistor to the left of R_{35} should be labelled R_{37} .

The accompanying diagram shows the corrected component mounting plan of busboard 1 (Fig. 6 on p. 33). Note the placement of points M and N, and the connections between the tuner input terminals and points E and F.



Macrovision decoder/blanker

November 1988 11.48

The 158N4 LED, D5, may fail to light even when a video signal of sufficient amplitude is applied. This can be resolved by replacing the Type 7805 voltage regulator in position IC4 with an 7806 or 7808, which have the same pinning. The use of an 7808 requires R_{14} to be increased to 15 k Ω .

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